Version : 0.1

TECHNICAL SPECIFICATION

MODEL NO : PD040QX2

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Please contact PVI or its agent for further information.

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Dep	FAE	Panel Design	Electronic Design	Mechanical Design	Product Verification	Prepared By
Sign						

Revision History

Rev.	Issued Date	Revised Contents
0.1	December, 23, 2008	Preliminary

TECHNICAL SPECIFICATION

CONTENTS

Application

This data sheet applies to a color TFT LCD module, PD040QX2.This module applies to OA product(must use Analog to Digital driving board), which requires high quality flat panel display. If you must use in severe reliability environments, please don't extend over PVI's reliability test conditions.

2. Features

. Amorphous silicon TFT LCD panel with LED back-light unit

. Pixel in stripe configuration

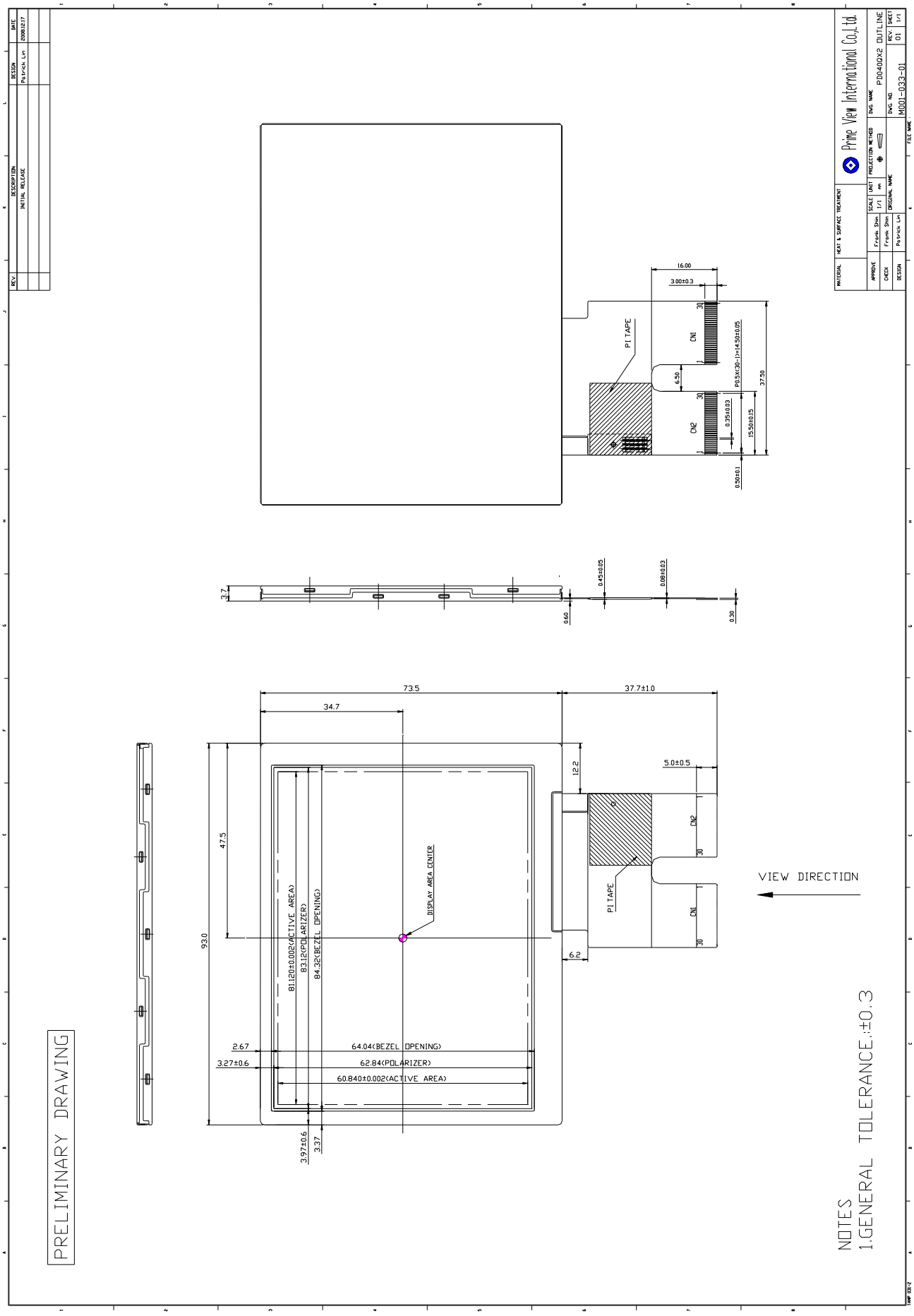
. Slim and compact, designed for O/A application

. TTL transmission interface

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	4 (diagonal)	inch
Display Format	320×(RGB)×240	dot
Active Area	81.12 (H)×60.84 (V)	mm
Pixel Pitch	0.2535(H)×0.2535 (V)	mm
Pixel Configuration	Stripe	
Display Colors	16.7M	
Surface Treatment	Anti-Glare +EWV	
Back-light	12-LEDs	
Outline Dimension	93.00(W)×73.50 (H)×3.7 (D)(typ.)	mm
Weight	TBD	g
Display mode	Normally white	
Gray scale inversion direction	6 (ref to Note 14-1)	o'clock

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

FPC Down Connect, 30 Pins, Pitch: 0.5 mm

CN 1

Pin No.	Symbol	Function	Remark
1	D27(B7)	Blue Data	Note 5-1
2	D26(B6)	Blue Data	
3	D25(B5)	Blue Data	
4	D24(B4)	Blue Data	
5	D23(B3)	Blue Data	
6	D22(B2)	Blue Data	
7	D21(B1)	Blue Data	
8	D20(B0)	Blue Data	
9	GND	Digital ground	
10	D17(G7)	Green Data	Note 5-1
11	D16(G6)	Green Data	
12	D15(G5)	Green Data	
13	D14(G4)	Green Data	
14	D13(G3)	Green Data	
15	D12(G2)	Green Data	
16	D11(G1)	Green Data	
17	D10(G0)	Green Data	
18	GND	Digital ground	
19	D07(R7)	Red Data	Note 5-1
20	D06(R6)	Red Data	
21	D05(R5)	Red Data	
22	D04(R4)	Red Data	
23	D03(R3)	Red Data	
24	D02(R2)	Red Data	
25	D01(R1)	Red Data	
26	D00(R0)	Red Data	
27	GND	Digital ground	
28	VEE	Negative power for gate driver	Note 5-8
29	VCC2	Digital power supply for gate driver	Note 5-9
30	VGG	Positive power for gate driver	Note 5-10

CN 2

Pin No.	Symbol	Function	Remark
1	VLED	Voltage for LED	
2	GLED2	LED ground	
3	GLED2	LED ground	
4	GND	Digital ground	
5	VCOM	Voltage for common electrode	Note 5-7
6	VSET	Externally/Internally gamma voltage setup	Note 5-11
7	VDDA	Analog power supply for source driver	Note 5-2
8	V10	Gamma correction voltage 10	
9	V9	Gamma correction voltage 9	
10	V8	Gamma correction voltage 8	
11	V7	Gamma correction voltage 7	
12	V6	Gamma correction voltage 6	
13	V5	Gamma correction voltage 5	
14	V4	Gamma correction voltage 4	
15	V3	Gamma correction voltage 3	
16	V2	Gamma correction voltage 2	
17	V1	Gamma correction voltage 1	
18	VSSA	Analog ground for source drive	
19	L/R	Left/Right control for source driver	Note 5-12
20	U/D	Up/Down control for gate driver	Note 5-12
21	GND	Digital ground	
22	VCC1	Digital power supply for source driver	Note 5-6
23	RESETB	Hardware global reset	
24	SPDA	Serial port data input/output	
25	SPCK	Serial port clock	
26	SPENA	Serial port data enable signal	
27	DEN	Input data enable control	Note 5-5
28	HS	Horizontal sync input	Note 5-3
29	VS	Vertical sync input	Note 5-4
30	CLK	Clock signal. Latching data at the rising edge	

Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.

If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.

If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to GND.

Note 5-2 : VDDA Typ. = 9.6V

Note 5-3 : Horizontal sync input in digital RGB mode and CCIR601 mode.
(Short to GND if not used)

Note 5-4 : Vertical sync input in digital RGB mode and CCIR601 mode.
(Short to GND if not used)

Note 5-5 : The SYNC(HS+VS) Mode and DEN mode are supported. If DEN signal is fixed low, SYNC Mode is used. Otherwise , DEN mode is used.

Note 5-6 : VCC1 Typ. = 3.3V

Note 5-7 : VCOM Typ.＝3.68V

Note 5-8 : VEE Typ. = -8V

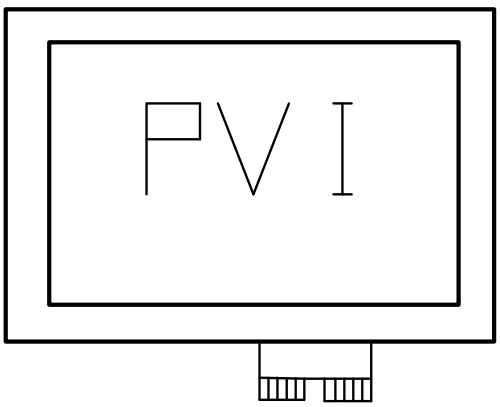
Note 5-9 : VCC2 Typ.＝3.3V

Note 5-10 : VGG Typ. =17V

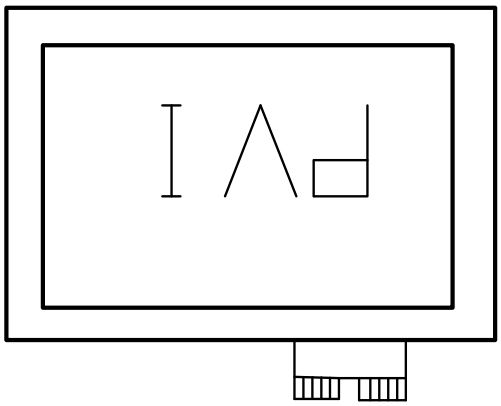
Note 5-11 :If.VSET="H",the gamma correction voltage generated externally.

Note 5-12 : The definition of L/R , U/D

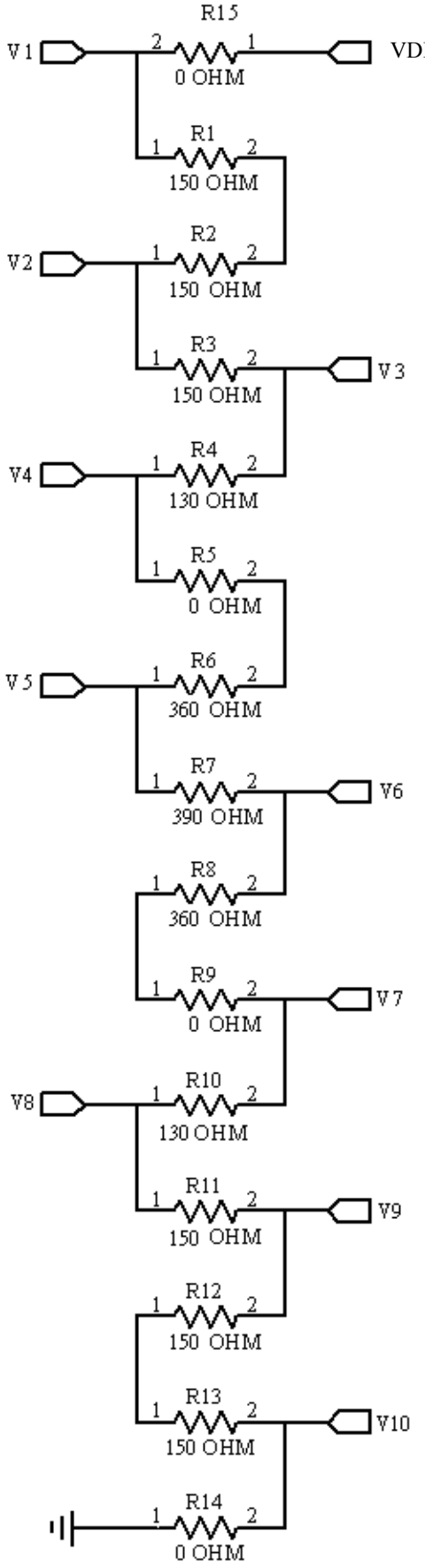
U/D CN2(PIN20)= Low
L/R CN2(PIN19)=High



U/D CN2(PIN20)= High
L/R CN2(PIN19)=Low



Typical Application Circuit (When VDDA = 9.6V)



6. Absolute Maximum Ratings:

GND=0V, Ta=25℃

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	VCC2	-0.3	6.0	V	
	VCC1	-0.3	7.0	V	
	VDDA	-0.3	13.5	V	
	VGG	-0.3	40.0	V	
	VGG-VEE	-0.3	40.0	V	
	VEE	-20	0.3	V	
Storage Temperature	Tst	TBD	TBD	℃	
Operation Temperature	Top	TBD	TBD	℃	

7. Electrical Characteristics

7-1) Recommended Operating Conditions:

VSSA=GND=0V, Ta=25℃

Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
Supply Voltage for Source Driver	VCC1	2.7	3.3	3.6	V	Note 7-1
	VDDA	6.5	9.6	13.5	V	
Supply Voltage for Gate Driver	VGG	-	17	-	V	
	VEE	-	-8	-	V	
	VCC2	2.7	3.3	3.6	V	
VCOM Voltage	VCOM	-	TBD	-	V	
Digital Input Voltage	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	V_{IL}	0	-	0.3 V_{CC}	V	

Note 7-1 : To test the current dissipation of V_{CC}, using the “color bars” testing pattern shown as below.

1	2	3	4	5	6	7	8

1. White
2. Yellow
3. Cyan
4. Green
5. Magenta
6. Red
7. Blue
8. Black

I_{DD} current dissipation testing pattern

7-2) Recommended Driving Condition for Back Light Ta=25℃

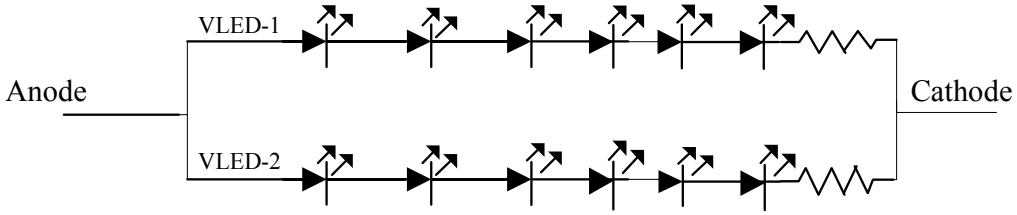
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
Supply voltage of LED backlight	V_{LED}	-	-	(21)	V	Note 7-2
Supply current of LED backlight	I_{LED}	-	20	-	mA	Note 7-3
Backlight Power Consumption	P_{LED}	-	-	840	mW	Note 7-2、7-4

Note 7-2 : I_{LED}= 20mA,constant current

Note 7-3 : The LED driving condition is defined for each LED module. (6 LED Serial)

Input current = 20mA * 2 = 40mA

Note 7-4 : $P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2}$



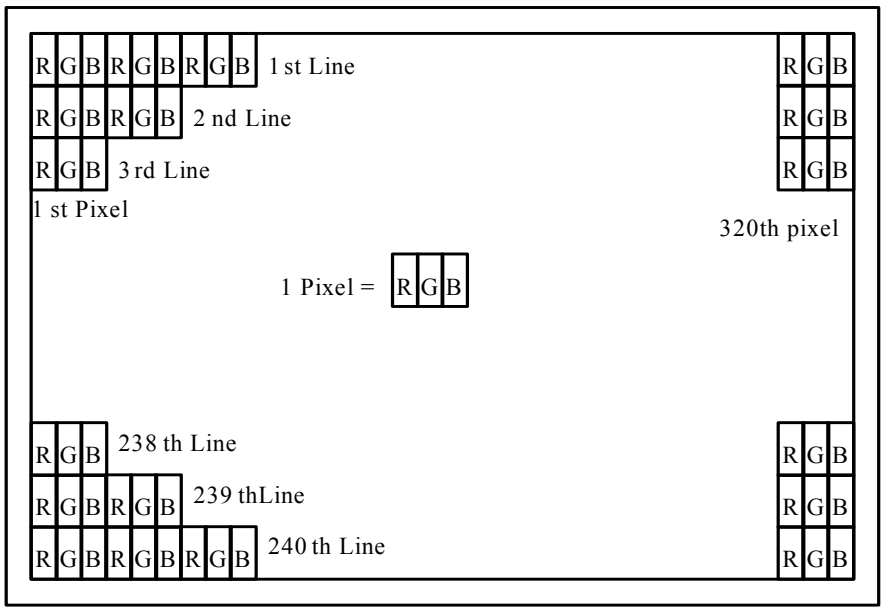
7-3) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	IGG	VGG= 17V	TBD	TBD	mA	
Supply Current for Gate Driver (Low level)	IEE	VEE= -8V	TBD	TBD	mA	
Supply Current for Gate Driver (Digital)	ICC2	VCC2= 3.3V	TBD	TBD	mA	
Supply Current for Source Driver (Digital)	ICC1	VCC1= 3.3V	TBD	TBD	mA	
Supply Current for Source Driver (Analog)	IDD	VDD= 9.6V	TBD	TBD	mA	
LCD Panel Power Consumption	-	-	TBD	TBD	mW	Note 7-5
Backlight LED Power Consumption	P_{LED}	-	TBD	TBD	mW	Note 7-6
Total Power Consumption	-	-	TBD	TBD	mW	

Note 7-5: The power consumption for backlight is not included.

Note 7-6: Back light power consumption is calculated by $I_L \times V_L$.

8. Pixel Arrangement



9. Display Color and Gray Scale Reference

Color		Input Color Data																									
		Red								Green								Blue									
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Magent	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Red	Red	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Darker																										
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		
	Brighte																										
	Red	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Green	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0		
	Darker																										
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		
	Brighte																										
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0		
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0		
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
Blue	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		
	Darker																										
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		
	Brighte																										
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1		
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0		
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		

10. Operation description

10-1) SPI Register Description

Register	Test	Address				Data							
Name	RW	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	△	△	△	△	△	PSC	STB	RESETB
						△	△	△	△	△	0	0	1
R1	0	0	0	0	1	△	△	△	RESL1	RESL0	IF2	IF1	IF0
						△	△	△	1	0	0	0	1
R2	0	0	0	1	0	△	△	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
						△	△	0	0	0	0	0	0
R3	0	0	0	1	1	△	△	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
						△	△	0	0	0	0	0	0
R4	0	0	1	0	0	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
						1	0	0	1	0	0	0	1
R5	0	0	1	0	1	AUTO_DP	DSIP_ON	A_TIME1	A_TIME.	B_TIME2	B_TIME1	B_TIME0	1
						1	0	0	1	0	1	0	1

△ RW must always keep low

Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	reserved	reserved	RESETB
Default	-	-	-	-	-	-	-	1

RESETB: Global reset.
RESETB="L", global reset the whole chip.
RESETB="H", Normal operation.

Register R1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	RESL1	RESL0	IF2	IF1	IF0
Default	-	-	-	1	0	0	0	1

Register R1 setting

RESL [1:0]:Display resolution selection

RESL1	RESL0	Resolution
0	0	320×RGB×240
0	1	reserved
1	0	reserved
1	1	reserved

Display resolution selection

IF[2:0]:Data input mode selection

IF2	IF1	IF0	Data input format	operating freq
0	0	0	reserved	reserved
0	0	1	24-bis parallel RGB	25.175MHz(MAX)
0	1	0	reserved	reserved
0	1	1	reserved	reserved
1	0	0	reserved	reserved
1	0	1	reserved	reserved
1	1	0	reserved	reserved
1	1	1	reserved	reserved

Data input mode selection

Register R2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
Default	-	-	0	0	0	0	0	0

Register R2 setting

STHD[5:0]:adjust start pulse position by dot

STHD5	STHD4	STHD3	STHD2	STHD1	STHD0	STH position sdjust	Unit
0	0	0	0	0	0	0	TCPH
0	0	0	0	0	1	+1	TCPH
0	0	0	0	1	0	+2	TCPH
0	0	0	0	1	1	+3	TCPH
0	0	0	1	0	0	+4	TCPH
0	0	0	1	0	1	+5	TCPH
0	0	0	1	1	0	+6	TCPH
0	0	0	1	1	1	+7	TCPH
0	1	1	0	0	0	+24	TCPH
0	1	1	0	0	1	+25	TCPH
0	1	1	0	1	0	+26	TCPH
0	1	1	0	1	1	+27	TCPH
0	1	1	1	0	0	+28	TCPH
0	1	1	1	0	1	+29	TCPH
0	1	1	1	1	0	+30	TCPH
0	1	1	1	1	1	+31	TCPH
1	0	0	0	0	0	-1	TCPH
1	0	0	0	0	1	-2	TCPH
1	0	0	0	1	0	-3	TCPH
1	0	0	0	1	1	-4	TCPH
1	0	0	1	0	0	-5	TCPH
1	0	0	1	0	1	-6	TCPH
1	0	0	1	1	0	-7	TCPH
1	0	0	1	1	1	-8	TCPH
0	0	0	0	0	0	-25	TCPH
0	0	0	0	0	1	-26	TCPH
0	0	0	0	1	0	-27	TCPH
0	0	0	0	1	1	-28	TCPH
0	0	0	1	0	0	-29	TCPH
0	0	0	1	0	1	-30	TCPH
0	0	0	1	1	0	-31	TCPH
0	0	0	1	1	1	-32	TCPH

Register R3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
Default	-	-	0	0	0	0	0	0

Register R3 setting

STVP3	STVP2	STVP1	STVP0	STV position adjust	Unit
0	0	0	0	0	T_H
0	0	0	1	+1	T_H
0	0	1	0	+2	T_H
0	0	1	1	+3	T_H
0	1	0	0	+4	T_H
0	1	0	1	+5	T_H
0	1	1	0	+6	T_H
0	1	1	1	+7	T_H
1	0	0	0	-1	T_H
1	0	0	1	-2	T_H
1	0	1	0	-3	T_H
1	0	1	1	-4	T_H
1	1	0	0	-5	T_H
1	1	0	1	-6	T_H
1	1	1	0	-7	T_H
1	1	1	1	-8	T_H

Adjust first line position by line

FRAD[1:0]:Odd frame or Even frame advance control

FRAD1	FRAD0	Advance Frame	Notes
0	0	reserved	reserved
0	1	reserved	reserved
1	0	Even Frame	Odd frame Tstv=STVP setting + 1H
1	1	Reserve	Reserve

Odd frame or Even frame Advance control

Register R4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	VS_POL	HS_POL	NPC_SET	NPC_IN
Default	-	-	-	-	0	0	0	1

Register R4 setting

VS_POL: VS polarity setting.

VS_POL=L, negative polarity.

VS_POL=H, positive polarity.

Note: Please set the VS_POL=H when CCIR601 mode for video decoder SAA7114.
(Please refer the input timing of the "13-4) Data input format for CCIR601 Mode")

HS_POL: HS polarity setting.

HS_POL=L, negative polarity.

HS_POL=H, positive polarity.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.

NPC_SET=L, auto detection.

NPC_SET=H, define by NPC_IN.

NPC_IN: Define the NTSC/PAL mode by SPI.

NPC_IN=L, PAL.

NPC_IN=H, NTSC.

Register R5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTO_DP	SISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME2	B_TIME0	reserved
Default	1	0	0	1	0	1	0	-

Register R5 setting

AUTO_DP: When power on, select blank image display time decided by A_TIME (bit 5, 4) or DISP_ON (bit 6).
AUTO_DP ="L", Blank image display time decided by DISP ON (bit 6).
AUTO_DP ="H", Blank image display time decided by A TIME (bit 5, 4).

DISP_ON: When AUTO_DP (bit 7) = "L", and DISP_ON = "H", blank image display off, then display normal image.

A_TIME [1:0]: When AUTO_DP(bit 7) = "H". the blank image display time is decided by A_TIME
00: blank image display time is 8 VS time
01: blank image display time is 16 VS time
10: blank image display time is 32 VS time
11: blank image display time is 64 VS time

B_TIME [2:0]: When into STB mode. the blank image display time is decided by B_TIME.
000: blank image display time is 3 VS time.
001: blank image display time is 4 VS time.
010: blank image display time is 5 VS time.
011: blank image display time is 6 VS time.
100: blank image display time is 7 VS time.
101: blank image display time is 8 VS time.
110: blank image display time is 9 VS time.
111: blank image display time is 10 VS time.

10-2) Power ON/OFF sequence

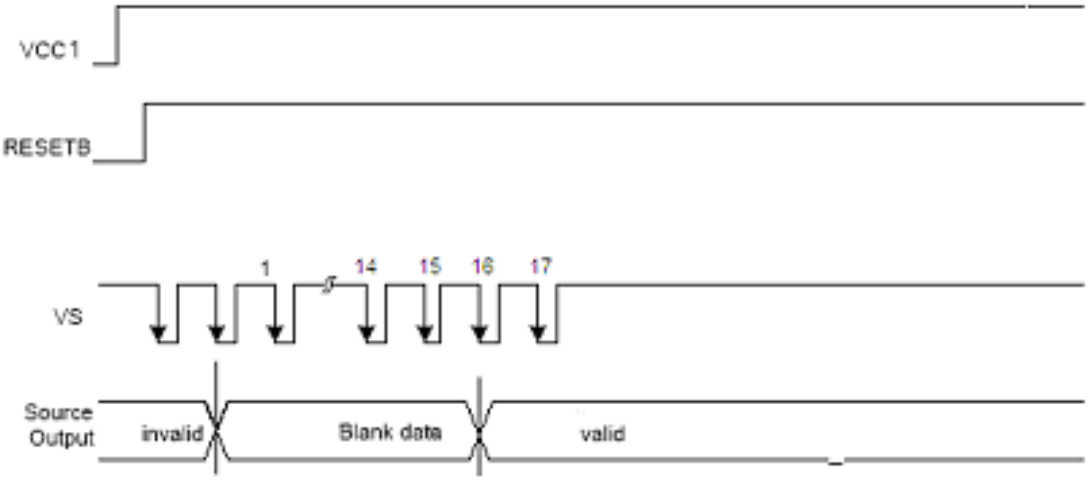
To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC1, GND → VDDA, VSSA → V1 to V10
Power OFF: V1 to V10 → VDDA, VSSA → VCC1, GND

10-3) Power ON Control

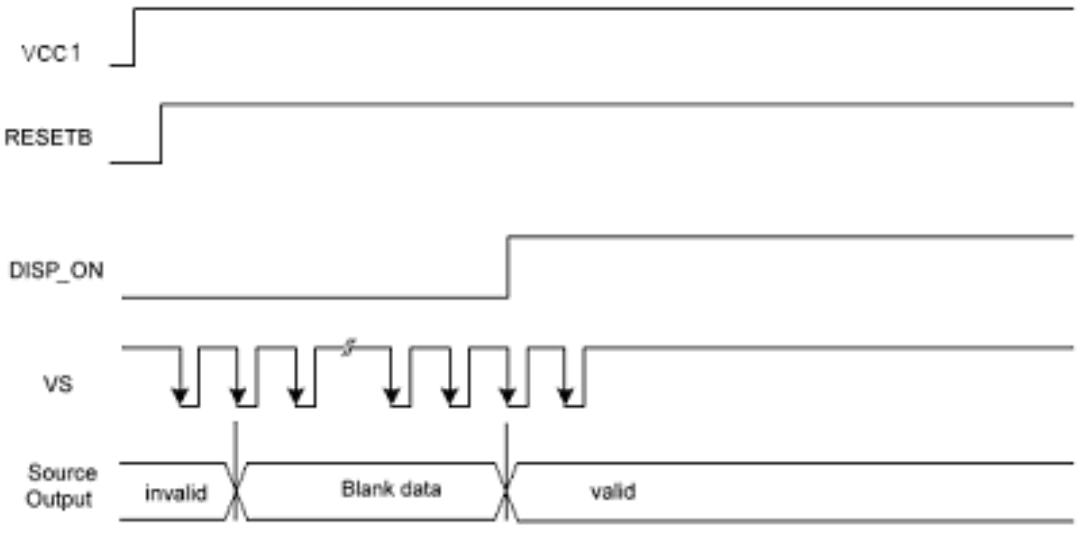
Source drive has a power ON sequence control function. There are two kinds of the mode. One is auto mode, and another is manual mode.

Auto Mode: When power is ON, blank data is outputted for 16-frames (default value) first, from the falling edge of the following VS signal. The blank data would be gray level 255 for normally white panel.
It can be defined in register R5 A_TIME1(bit 5) and A TIME0 (bit 4) when AUTO_DP(bit 7) = "H"



Power on control for Auto Mode

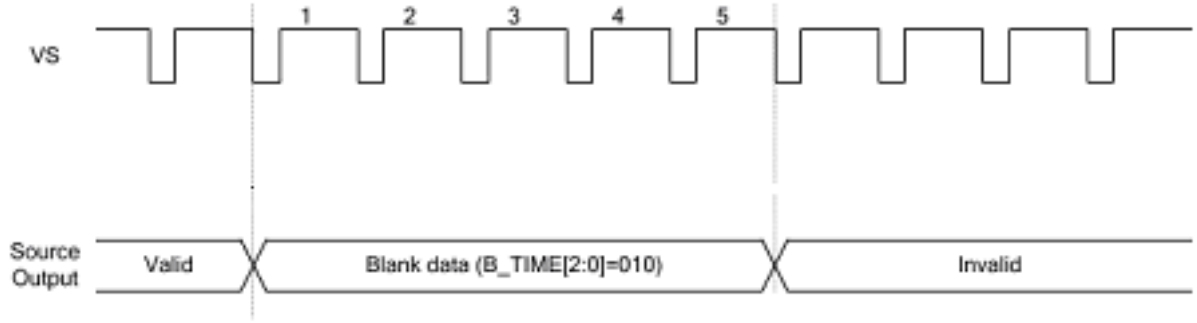
Manual Mode: When power is ON , you should set the register R5 AUTO_DP(bit 7) = "L" to stay at the manual mode. Blank data is outputted until the DISP_ON(bit 6) = H then display the normal image.



Power on control for Manual Mode

10-4) Standby ON/OFF Control

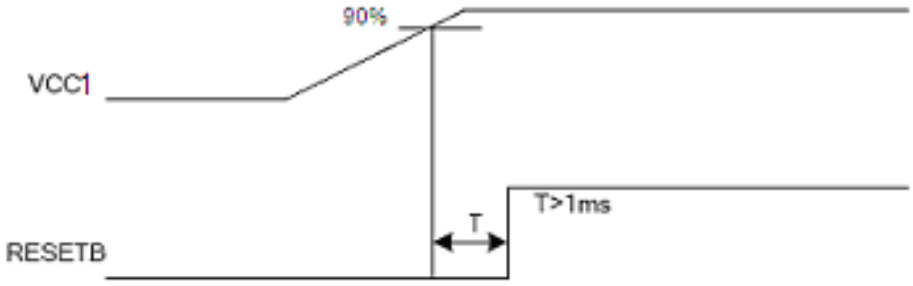
Source drive has a standby ON/OFF sequence control function. When STB pin is "L", blank data is outputted for 5-frames (default value) first, from the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white panel. It can be defined in register R5 B_TIME[2:0] to adjust the frame number of the blank data.



Standby ON/OFF Control

10-5) Reset when power on

Source drive is internally initialized by the global reset signal. RESETB. The reset input must be held for at least 1ms after power is stable.



RESETB control after power stable

11.AC Characteristics

11-1) SPI timing characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

11-2) Digital Parallel RGB interface

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	6.43	-	MHz
CLK period		T_{CPH}	-	155.62	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	408	-	T_{CPH}
HS pulse width		T_{WH}	5	30	-	T_{CPH}
HS-first horizontal data time		T_{HS}	36	68	99	T_{CPH}
DEN pulse width		T_{EP}	-	320	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

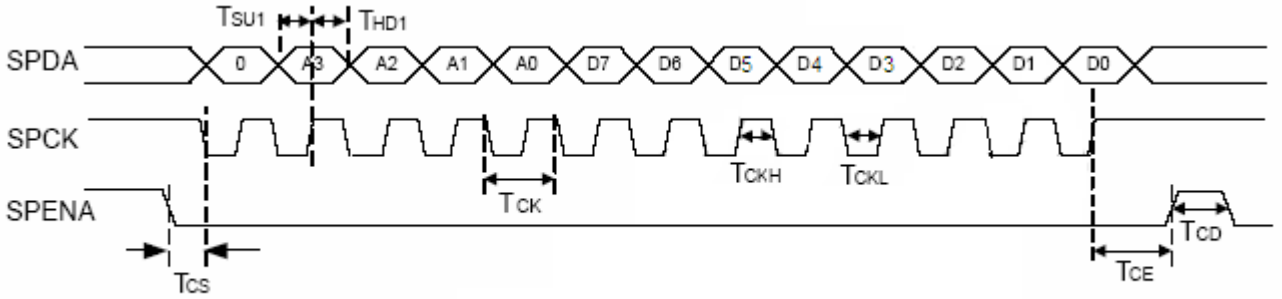
Note: When SYNC mode is used, 1st data start from 204th CLK after HS falling (when STHD[5:0]=000000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	26	-	T_{CPH}
CKV pulse width	T_{CKV}	-	24	-	T_{CPH}
HS-CKV time	T_1	-	16	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	25	-	T_{CPH}
STV setup time	T_{SUV}	-	10	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

12. Waveform

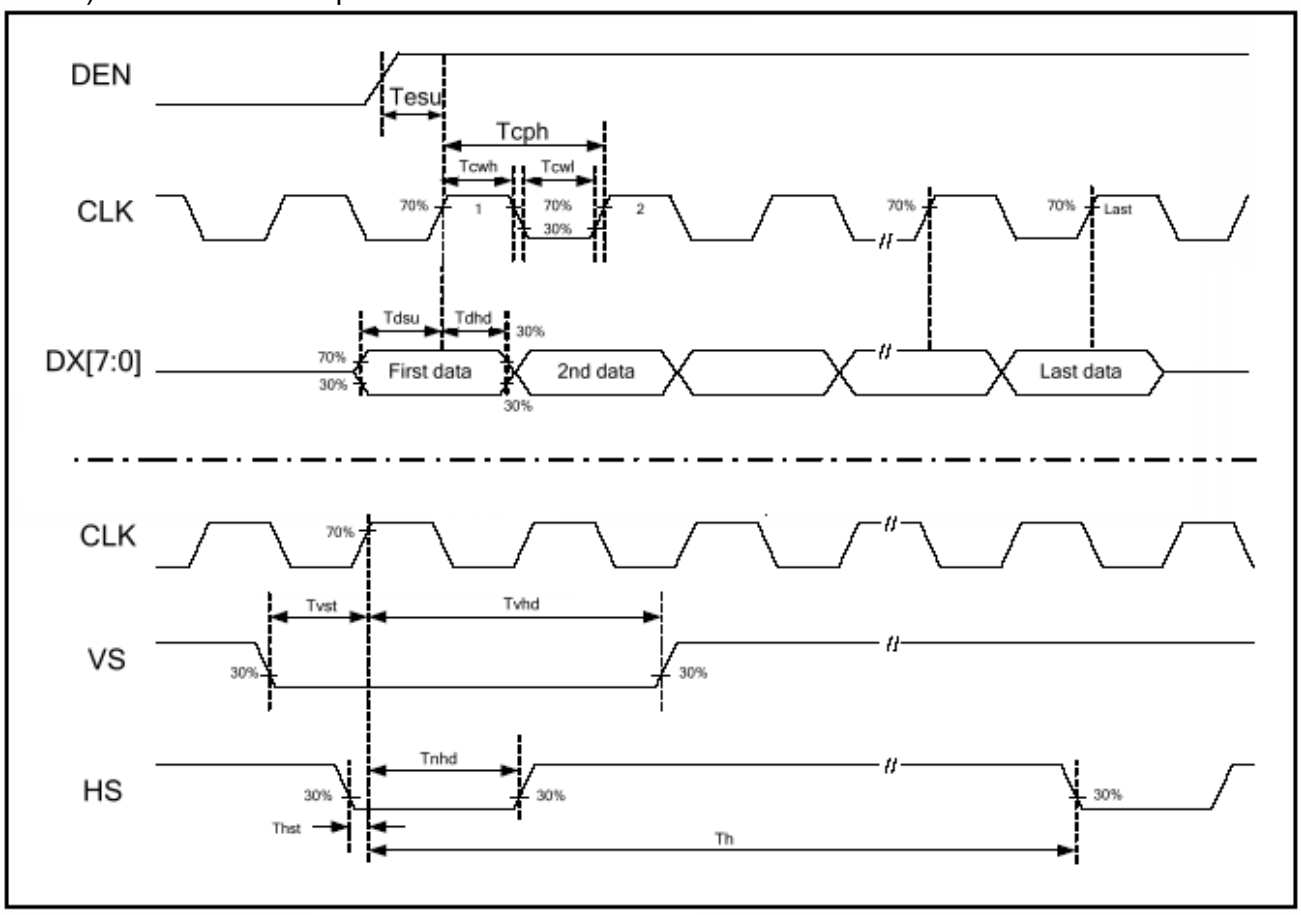
Timing Controller Timing Chart

12-1) SPI timing



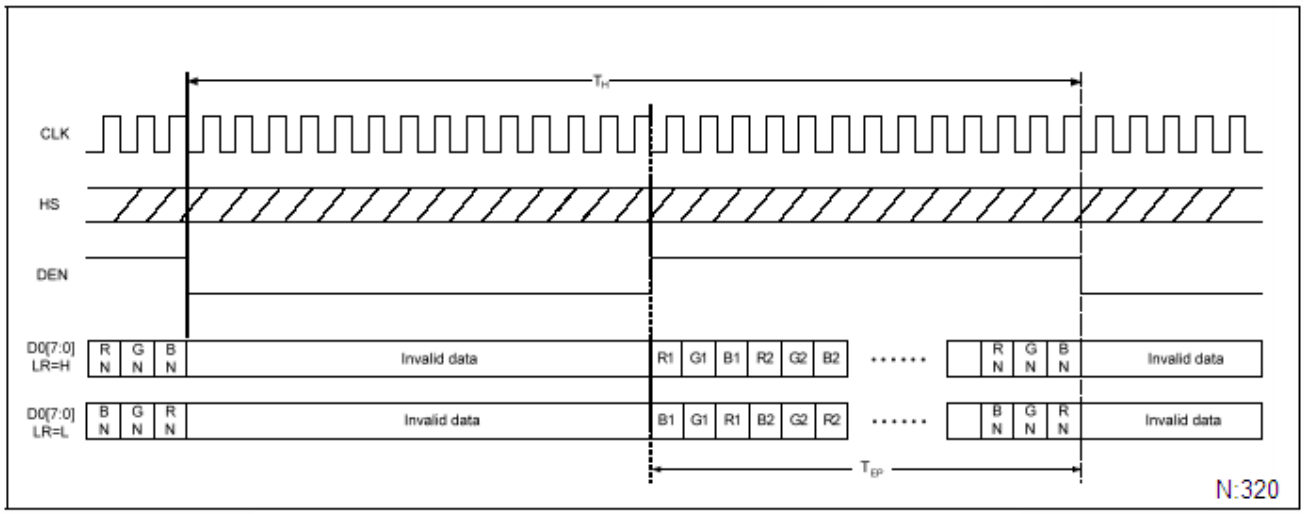
SPI timing

12-2) Clock and Data input waveforms

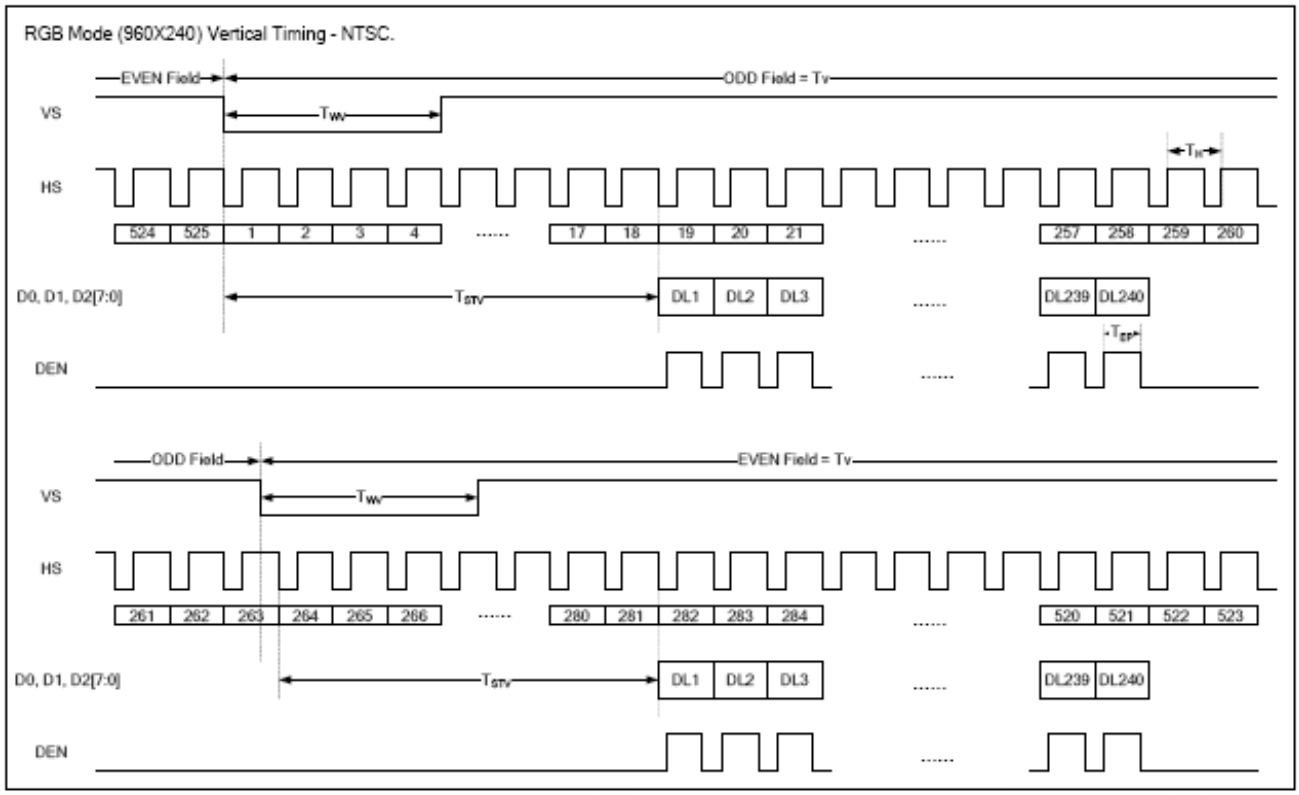


Clock and Data input waveforms.

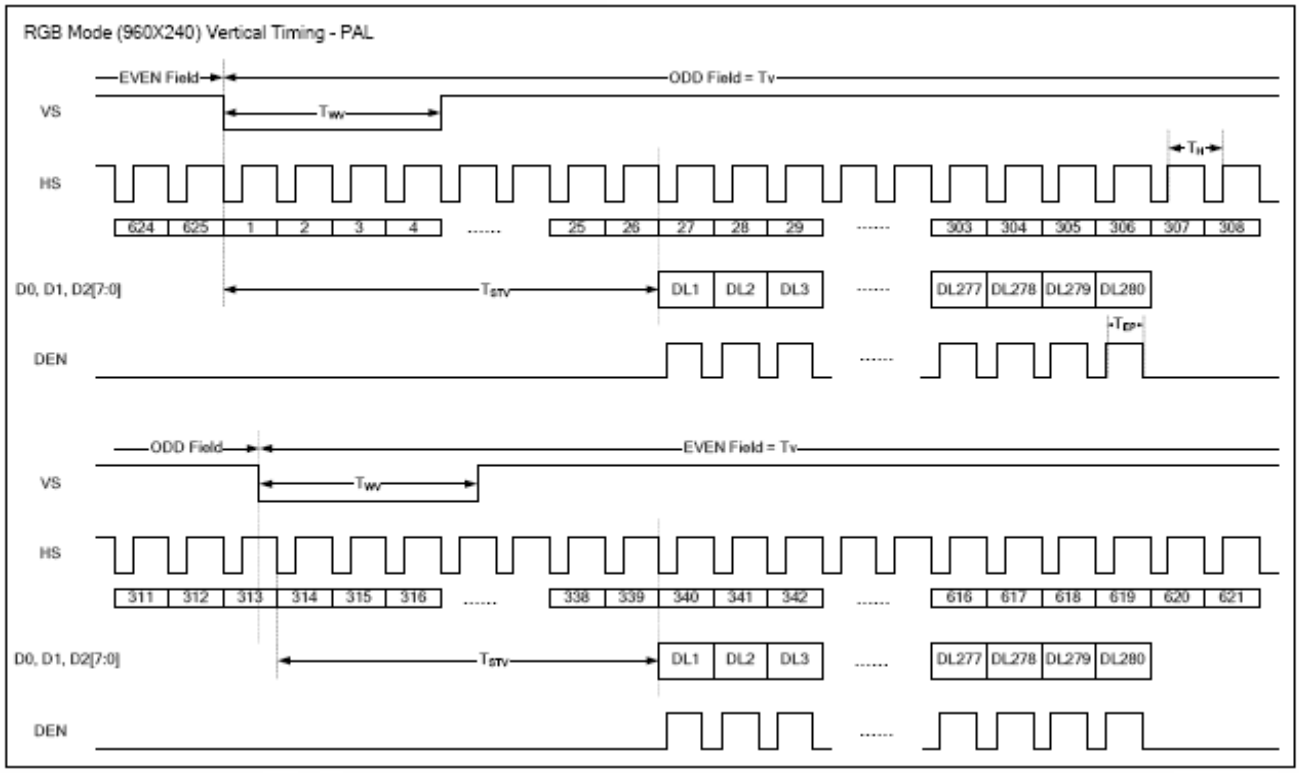
12-3) Data input format for RGB Mode



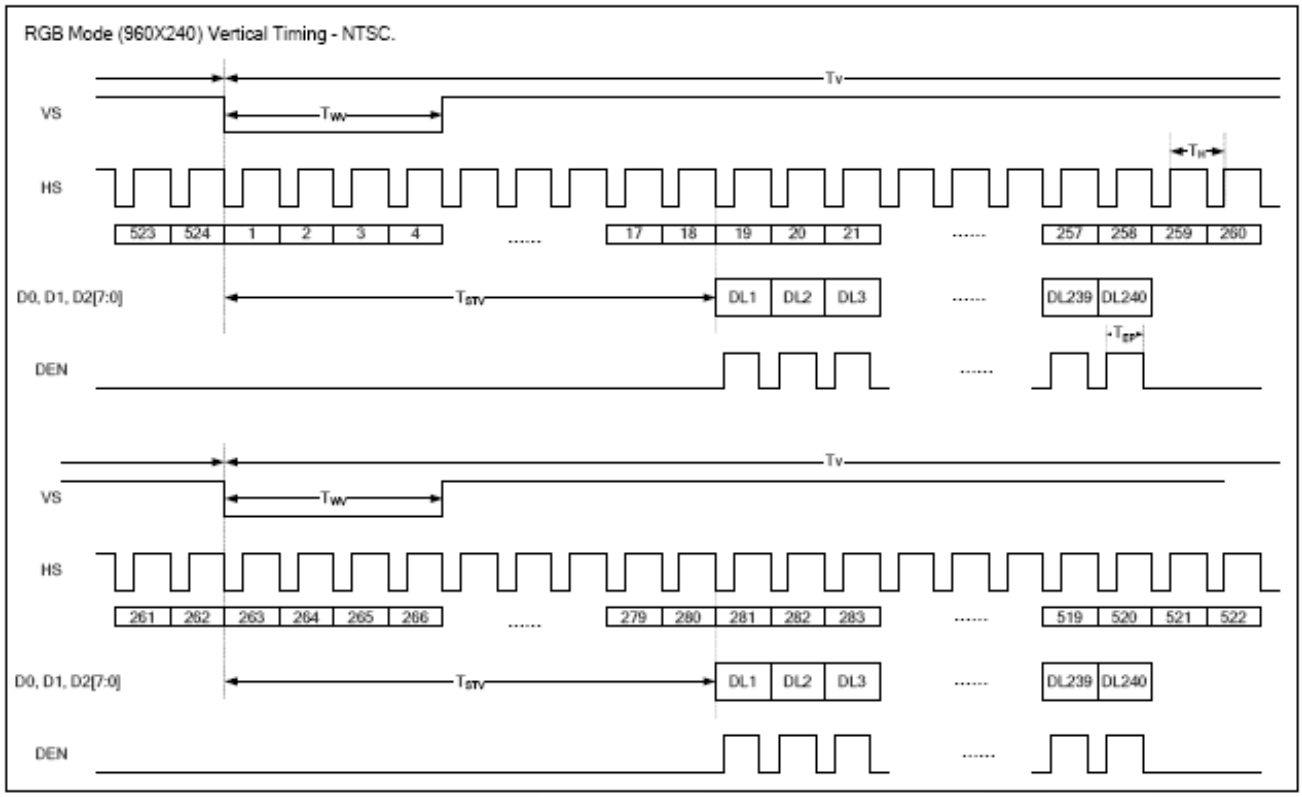
Parallel RGB Horizontal Data Format



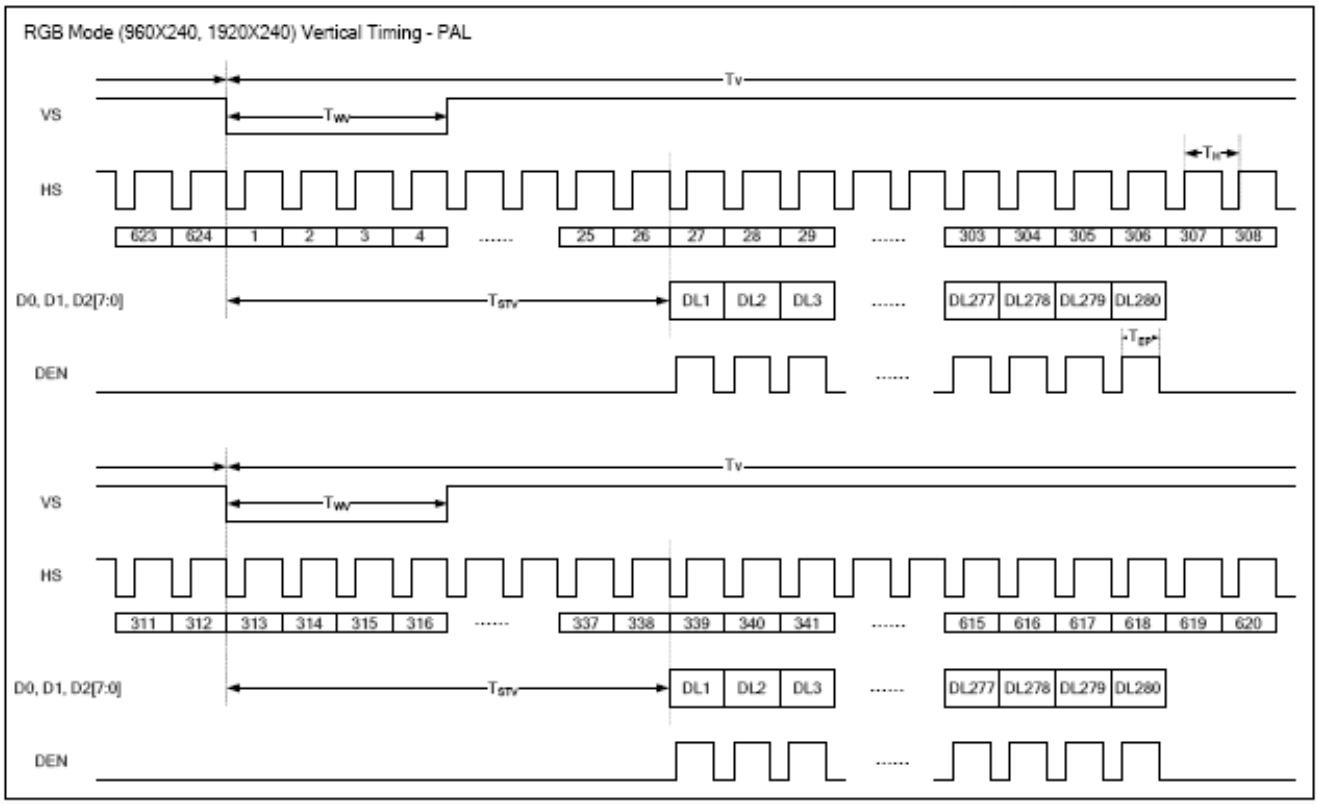
Digital RGB NTSC mode Vertical Data Format for 262.5T_H



Figu Digital RGB PAL mode Vertical Data Format for $312.5T_H$

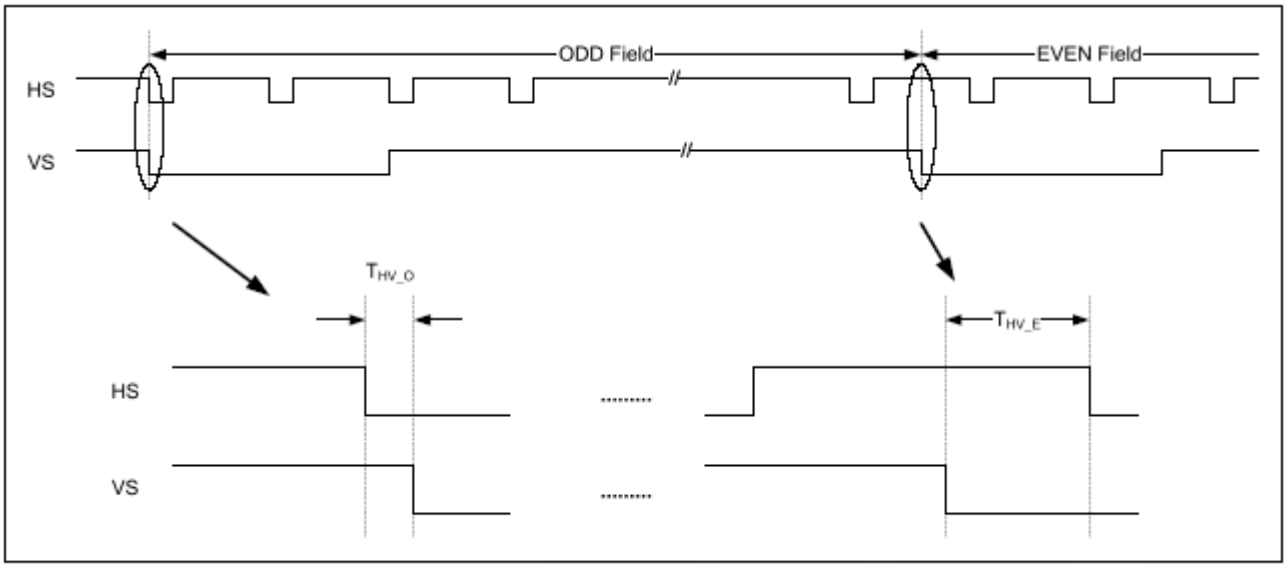


Digital RGB NTSC mode Vertical Data Format for $262T_H$



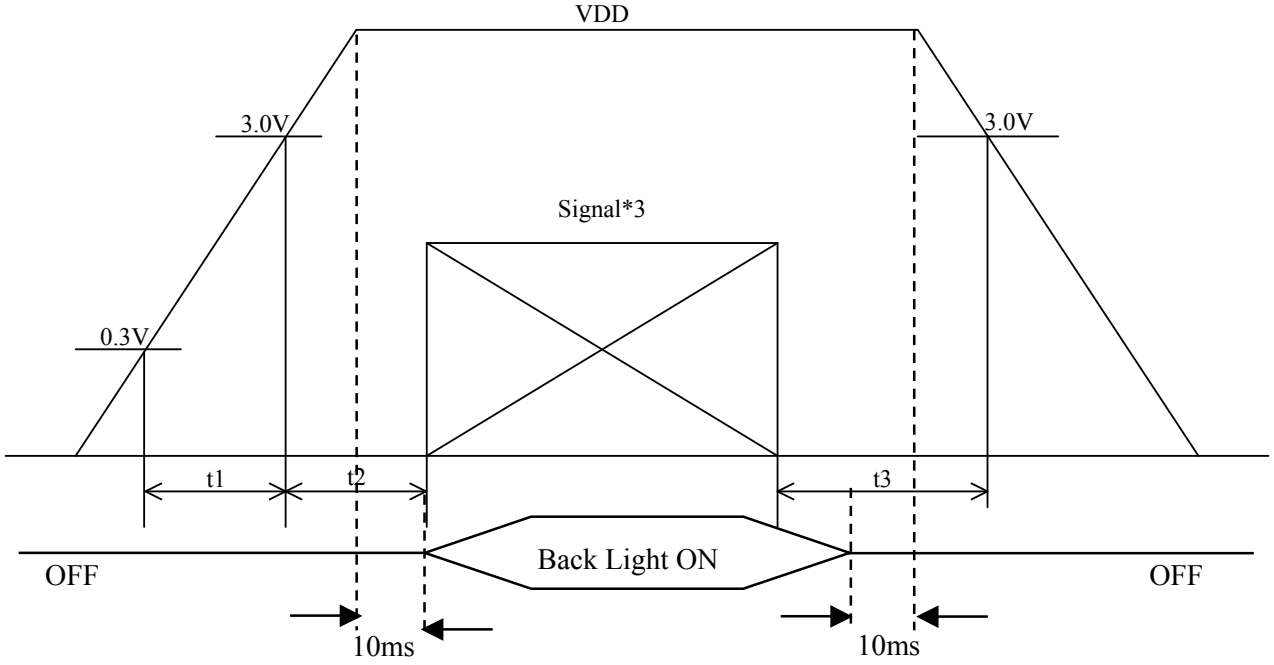
Digital RGB PAL mode Vertical Data Format for $312T_H$

12-4) The HS & VS timing of the ODD/EVEN field



Define the HSYNC to VSYNC timing for RGB mode

13.Power On Sequence



0＜t1≦20ms

0＜t2≦50ms

0＜t3≦1s

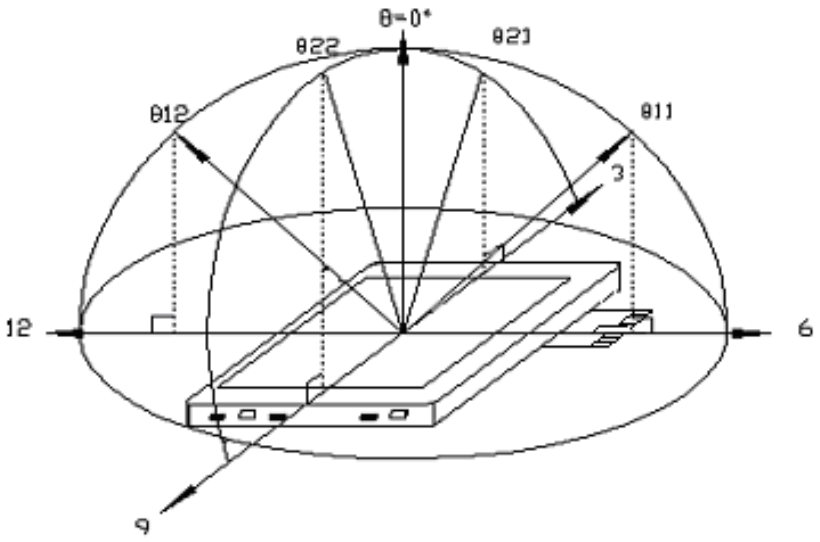
14. Optical Characteristics

14-1) Specification: Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ21, θ22	CR≧10	(75)	(80)	---	deg	Note 14-1
	Vertical	θ12		(45)	(50)	---	deg	
		θ11		(55)	(60)	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	(200)	(400)	---		Note 14-2
Luminance		L	θ=0°	(800)	(1000)	---	cd/㎡	
White Chromaticity		x	θ=0°	(0.26)	(0.30)	(0.34)		
		y	θ=0°	(0.29)	(0.33)	(0.37)		
Response time	Rise	Tr	θ=0°	---	15	30	ms	Note 14-3
	Fall	Tf		---	25	50	ms	
Uniformity		U	-	(75)	(80)	---	%	Note 14-5
Cross Talk Ratio		CTK	-	---	---	3.5	%	Note 14-6
LED Life Time			+25℃	(20000)	(25000)	---	hrs	Note 14-4

*():reference only

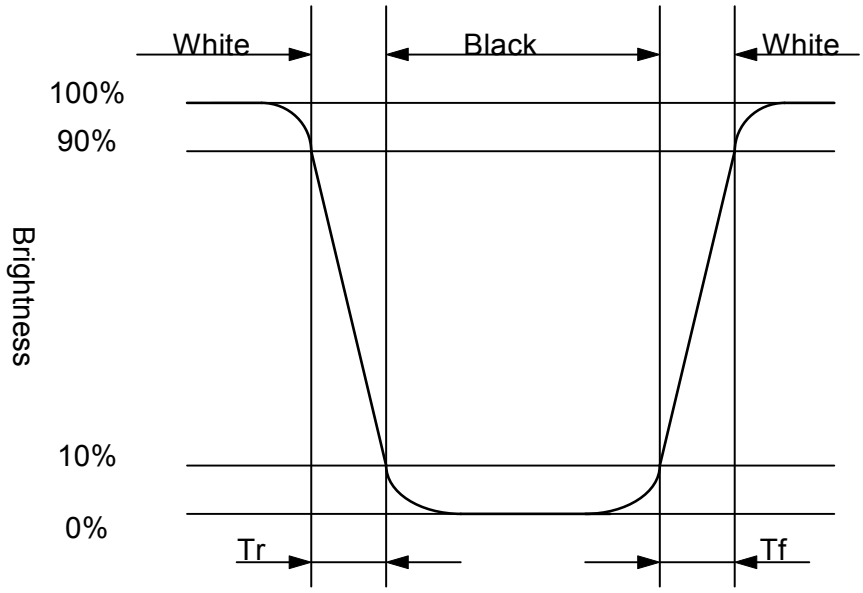
Note 14-1 : The definitions of viewing angles



Note 14-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.

Note 14-3 : The definition of response time :



Note 14-4 : The “LED Life time “ is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25℃ and I_{LED} =40mA

Note 14-5: The uniformity of LCD is defined as

U = The Minimum Brightness of the 9 testing Points / The Maximum Brightness of the 9 testing Points

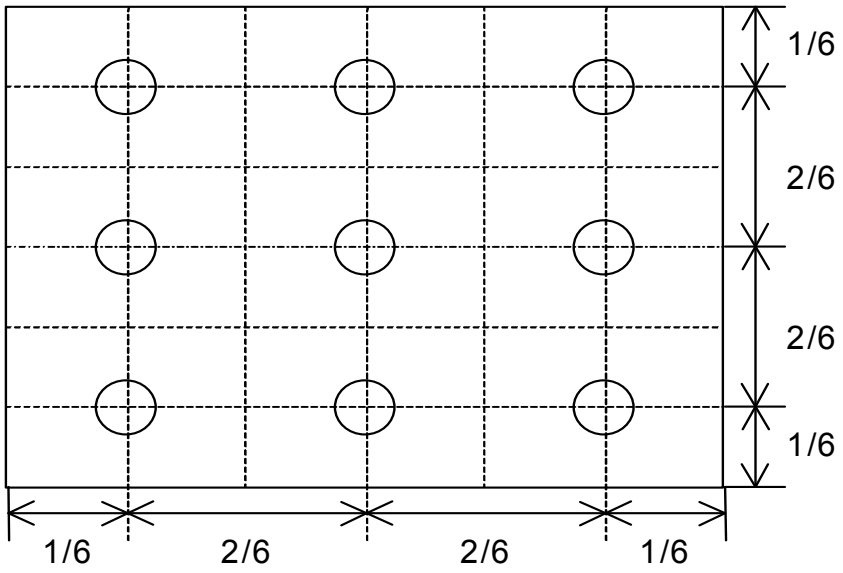
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The pattern is white



Note 14-6: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A

YB: Brightness of Pattern B

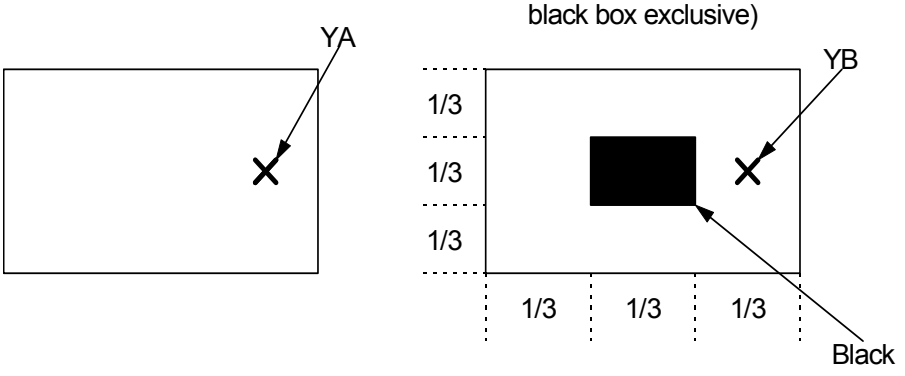
Luminance meter : BM 5A (TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Pattern A
(Gray Level 31)

Pattern B
(Gray Level 31, central black box exclusive)



✕: Measuring Point (A and B are at the same point.)

(Gray Level 0)

Measuring direction : Perpendicular to the surface of module

15. Handling Cautions

15-1) Mounting of module

a)Please power off the module when you connect the input/output connector.

b)Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

c)Protective film (Laminator) is applied on surface to protect it against scratches and dirt.

d)Please following the tear off direction as figure 15-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.

15-2) Precautions in mounting

a)When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b)Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c)TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d)Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

15-3) Adjusting module

a)Adjusting volumes on the rear face of the module have been set optimally before shipment.

b)Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

15-4) Others

a)Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b)Store the module at a room temperature place.

c)The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d)If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e)Observe all other precautionary requirements in handling general electronic components.

f)Please adjust the voltage of common electrode as material of attachment by 1 module.

15-5) Polarizer mark

The polarizer mark is to describe the direction of view angle film how to mach up with the rubbing direction.

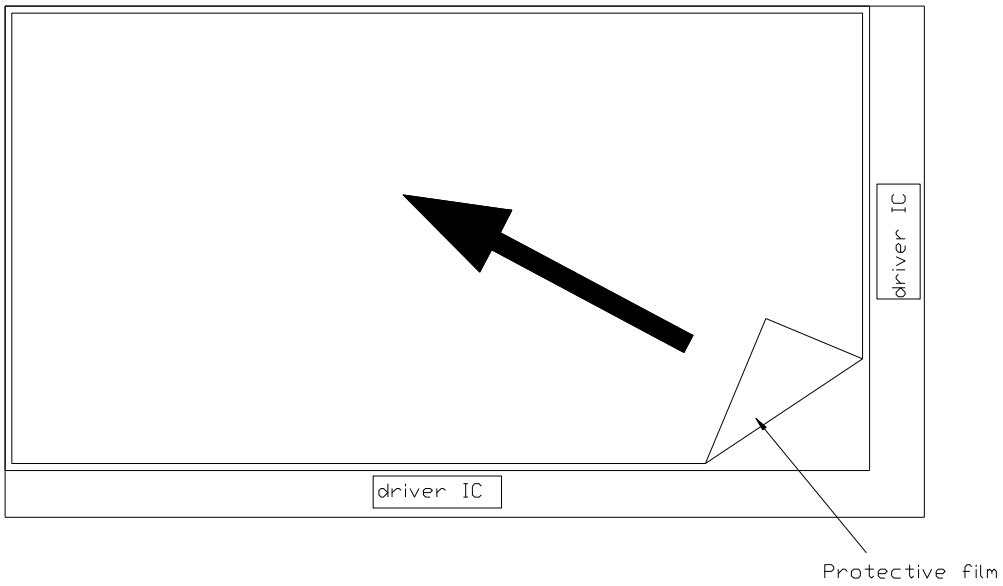
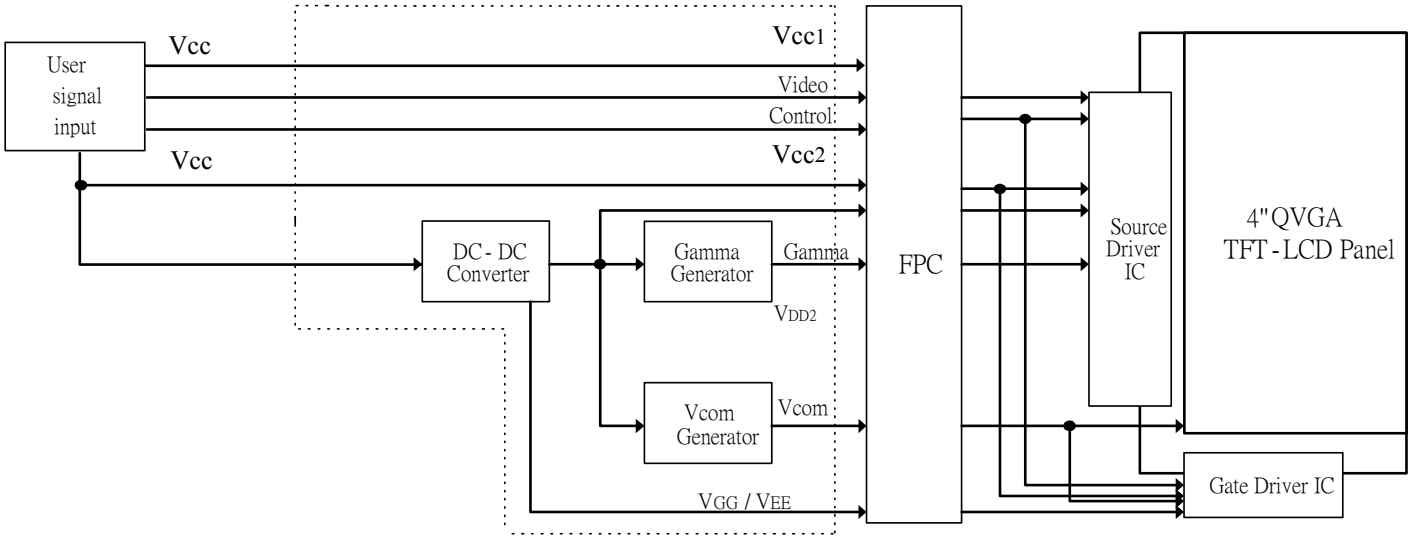


Figure 15 -1 the way to peel off protective film

16. Reliability Test

TBD

17. Block Diagram



18. Packing

TBD