HITACHI
Hitachi Displays, Ltd.

Date; May. 20, 2011

TENTATIVE

TECHNICAL DATA

TX43D90VM0BAA

CONTENTS

The information described in this technical specification is tentative and it is possible to be changed without prior notice.

RECORD OF REVISION

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APPLICATION

In the case of applying this product for such as control and safety device of transportation facilities (airplane, train, automobile, ship, etc), equipments aiming for rescue and security, and the other safety related devices which should secure higher reliability and safety, please make it sure that proper countermeasure such as fail-safe functions and enough system design for the protection are mandatory.

Please do not apply this product for equipments or devices which need exceedingly high reliability, such as aerospace applications, telecommunication facilities (trunk lines), nuclear related equipments or plants, and critical life support devices or applications. Usage style of this product is limited to Landscape mode. Optical characteristics mentioned in this spec. sheet is applied for only initial stage after delivery, and the characteristics will be changed by long time usage. Reliability of this product is secured as normal office use.

DESCRIPTION

The following specifications are applied to the following 17inch WXGA IPS-Pro-TFT module.

Note :The LED driver for the backlight unit is built in this module.

Product Name : TX43D90VM0BAA

GENERAL SPECIFICATIONS

Effective Display Area	: (H)369.60 × (V)221.76 [mm]
Number of Pixels	: (H)1,280 × (V)768 [pixels]
Pixel Pitch	: (H)0.28875 × (V)0.28875 [mm]
Color Pixel Arrangement	: R + G + B Vertical Stripe
Display Mode	: Transmissive Mode Normally Black Mode
Top Polarizer Type	: Anti-glare (Surface hardness: 2H)
Number of Colors	: 16,777,216 colors
Color Reproducibility	: NTSC-Ratio (77)%
Viewing Angle Range	: Super Wide Version (Horizontal & Vertical : 170°, CR ≥ 10)
Input Signal	: 1-channel LVDS (LVDS: Low Voltage Differential Signaling)
Back Light	: Edge Light Type with White LED
External Dimensions	: (H)400 × (V)258 × (t)(20.0) [mm]
Weight	: Typ. (1,700) [g]
RoHS	: Compliance

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENT ABSOLUTE MAXIMUM RATINGS

Item	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1)
Humidity	2)		2)		%RH	1)
Vibration	—	4.9 (0.5G)	—	9.8 (1.0G)	m/s^2	3)
Shock	—	29.4 (3G)	—	294 (30G)		4)
Corrosive Gas	Not Acceptable		Not Acceptable		—	—
Illumination at LCD Surface	—	50,000	—	50,000	lx	—

Notes 1) Temperature and Humidity should be applied to the center glass surface of TFT-LCD module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 60°C on the condition of operating.
Function of module is guaranteed in above operating temperature range, but optical characteristics is specified for only 25°C operating condition.

2) Ta ≤ 40°C ..... Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta > 40°C ..... Relative humidity should be lower than the moisture of the 85%RH at 40°C.

3) Frequency of the vibration is between 15Hz and 50Hz. (Remove the resonance point)

4) Pulse width of the shock is 3 ms.

1.2 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

(1) TFT-LCD Module

Vss=0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	6.5	V	—
Differential signal input voltage	V_{IL}	0	3.4	V	1)
Input Voltage for logic	V_I	-0.3	5.0	V	2)
Electrostatic Durability	V_{ESD0}	±100		V	3),5)
	V_{ESD1}	±8		kV	4),6)

Notes 1) It is applied to LVDS signal.

2) It is applied to except LVDS signal.

3) Discharge Coefficient: 200pF-0Ω, Environmental: 25°C-70%RH

4) Discharge Coefficient: 200pF-250Ω, Environmental: 25°C-70%RH

5) It is applied to I/F connector pins.

6) It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-Light

Vss=0V

Item	Symbol	Min.	Max.	Unit	Note
Input Voltage	V_{IN}	0	(15.0)	V	
ON/OFF Control Input Voltage	ON/OFF	0	5.0	V	
Analog Dimming Signal Voltage	V_{BC}	0	3.6	V	1)
PWM Dimming Signal Voltage	PWM	0	5.5	V	1)

Notes 1) These signals can't input at the same time.

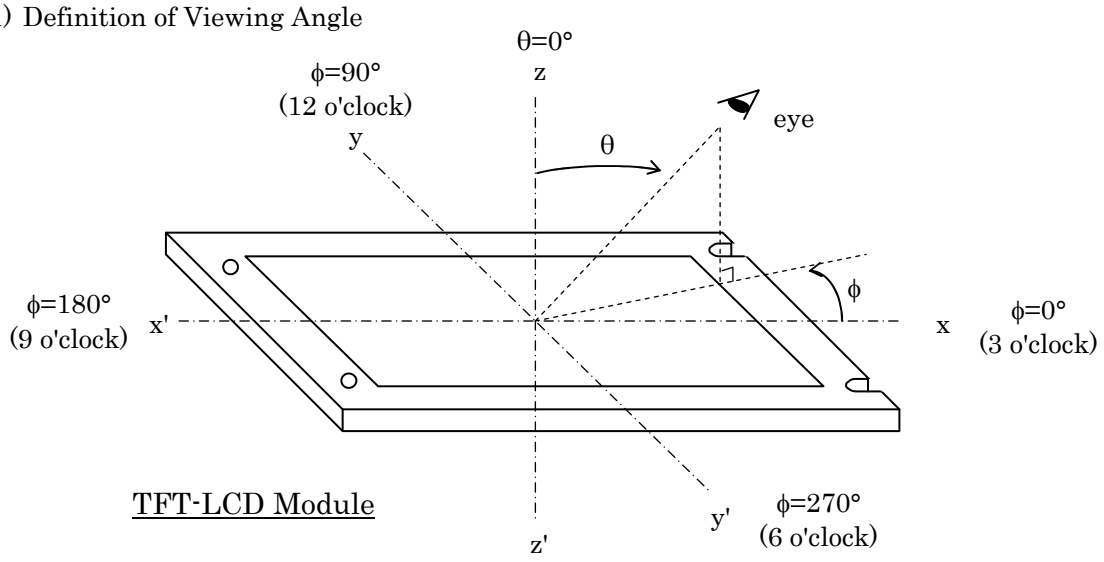
2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured when the LCD is set alone (apart from driving circuits and monitor cabinets) and under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.
The optical characteristics should be measured in a dark room or equivalent state.

Measuring equipment : KONICA MINOLTA: CS-2000 or equivalent.
Ambient Temperature =25±3°C, V_{DD}=5.0V, f_V=60Hz, Vin=12V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		700	1000	—	—	2)
Response Time	Rise	ton		—	(12)	(20)	ms	3)
	Fall	toff		—	(10)	(18)		
Brightness of white		Bwh		(420)	(500)	—	cd/m^2	—
Brightness uniformity		Buni		75	—	—	%	4)
Color Chromaticity (CIE)	Red	x	θ = 0° 1)	(0.620)	(0.650)	(0.680)	—	(Gray scale = 255)
		y		(0.299)	(0.329)	(0.359)		
	Green	x		(0.271)	(0.301)	(0.331)		
		y		(0.594)	(0.624)	(0.654)		
	Blue	x		(0.120)	(0.150)	(0.180)		
		y		(0.023)	(0.053)	(0.083)		
	White	x		(0.283)	(0.313)	(0.343)		
		y		(0.299)	(0.329)	(0.359)		

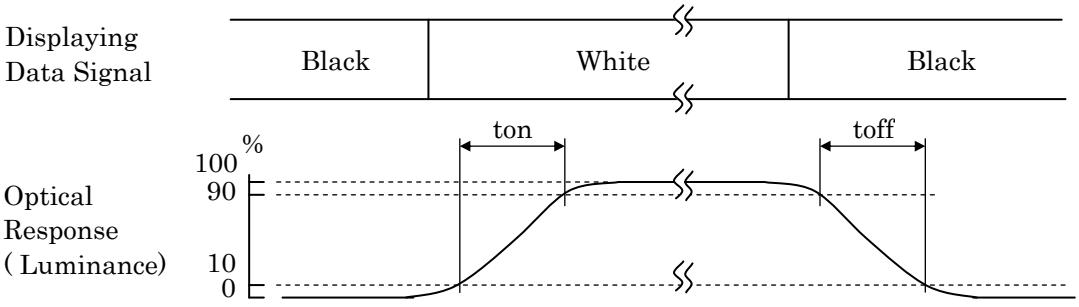
Notes 1) Definition of Viewing Angle



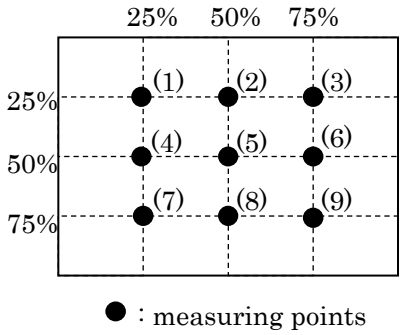
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level). The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \left(\frac{Bmin}{Bmax} \right) \times 100$$

where, Bmax = Maximum brightness
Bmin = Minimum brightness

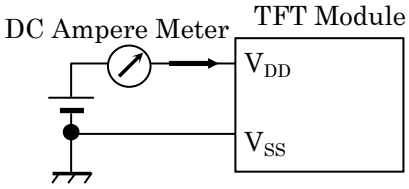
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD MODULE

Ta=25°C, V_{SS}=0V

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage		V_{DD}	4.5	5.0	5.5	V	—
Power Supply Current		I_{DD}	—	0.65	0.85	A	1),2),3)
Differential Input Voltage	High	V_{IH}	—	—	+100	mV	VCM=1.2V
For LVDS Receiver Threshold	Low	V_{IL}	-100	—	—	mV	VCM=1.2V
Frame Frequency		f_V	55	60	65	Hz	4)
One line scanning Frequency		f_H	44.8	47.1	52.3	kHz	4)
DCLK Frequency		f_{CLK}	65	66	73	MHz	4)

Notes 1) DC current at f_V=60Hz, f_{CLK}=66MHz and V_{DD}=5.0V



2) As this module contains fuse (1.6A), prepare current source that is enough for cutting current fuse (larger than 4.0A) or set a protection circuit when a trouble happens.
3) The picture on maximum current is white picture.
4) When at low frequency drive, flicker may appear on screen. Therefore, please verify the flicker level before system design.

3.2 BACK LIGHT

Ta=25°C

Item		Symbol		Min.	Typ.	Max.	Unit	Note
Input Voltage		V_{IN}		10.8	12.0	13.2	V	—
Input Current		I_{IN}		—	(1.2)	—	A	—
ON/OFF Control Voltage	ON	ON/OFF		2.5	—	5.0	V	B/L=ON
	OFF			0	—	0.8	V	B/L=OFF
Brightness Control Voltage		V_{BC}		1.0	—	3.6	V	1), 2)
PWM dimming signal Input Voltage		PWM	High	2.5	—	5.0	V	3)
			Low	0	—	0.8	V	
PWM Frequency		PWMf		140	150	(160)	Hz	

Dimensions in parentheses are reference value.

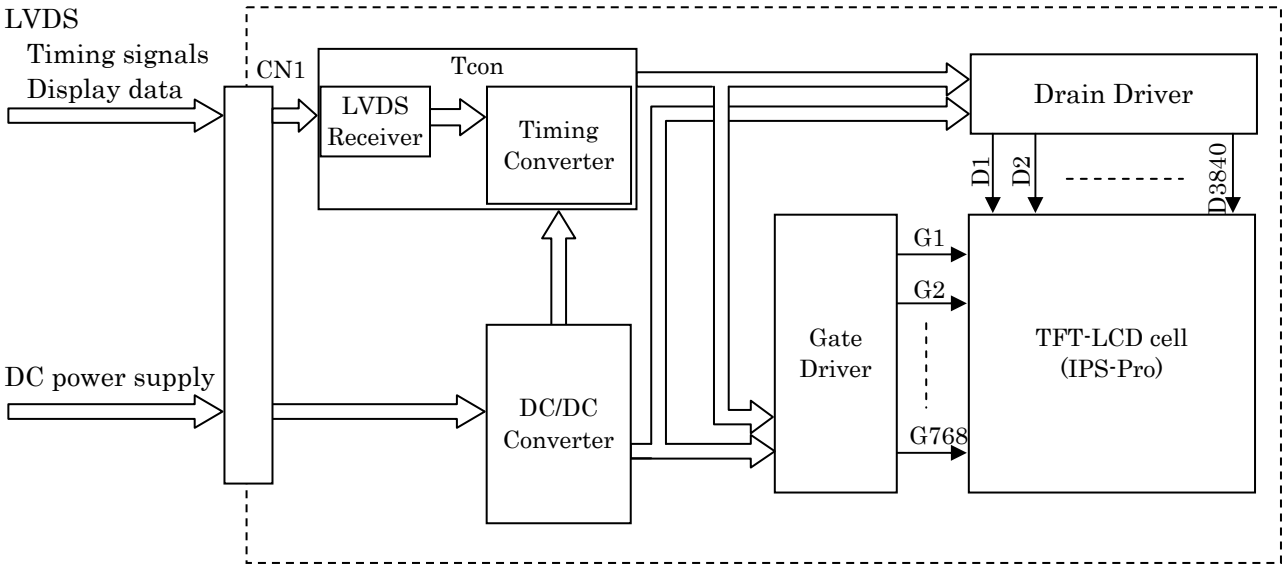
Notes 1) As for V_{BC}, it is recommendable to use more than 1.0V.
If V_{BC} is set less than 1.0V in which brightness becomes less than 20% to the maximum, display image may look unstable since relative change of brightness tends to become large by the slight drift of V_{BC}.

2) Brightness rises almost linearly by increaseing the V_{BC} in less than 3.0V.
However, brightness is saturated when V_{BC} exceeds 3.0V.

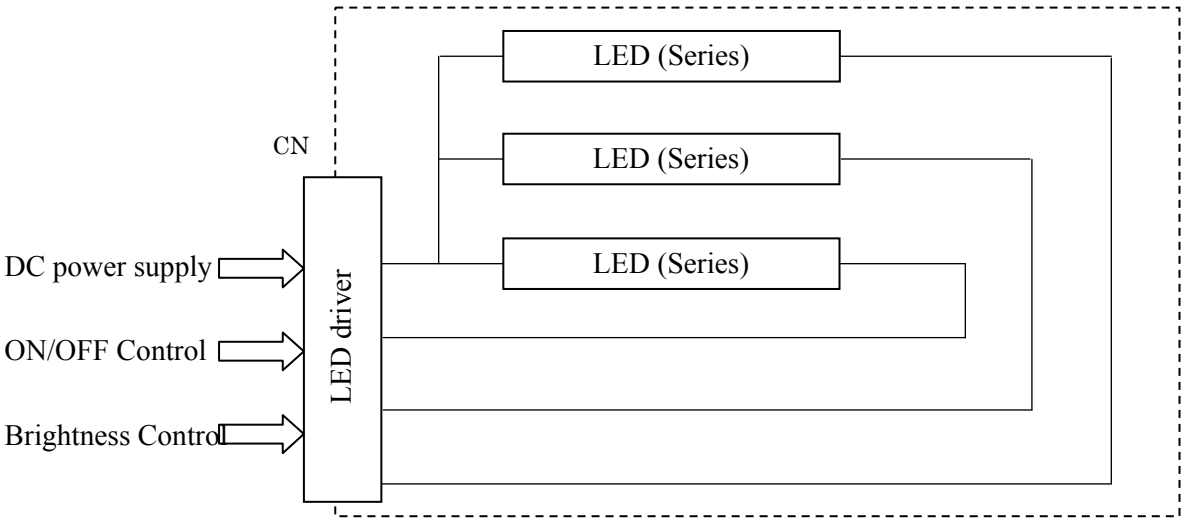
3) Brightness is almost proportional to the on-Duty ratio of PWM signal input.

4. BLOCK DIAGRAM

(1) TFT-LCD Module



(2) Back Light Unit



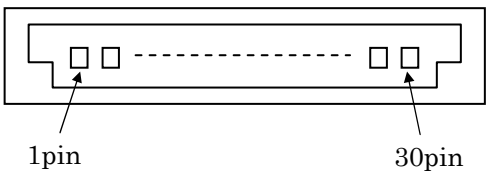
5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD MODULE

CN1: JAE: FI-X30SSLA-HF or Equivalent
(Matching connector: JAE: FI-X30HL or FI-X30C2L-NPB or Equivalent)

Pin No.	Symbol	Function	Note
1	VDD	Power Supply (+5.0V)	4)
2	VDD		
3	VDD		
4	VDD		
5	VSS	GND (0V)	1)
6	VSS		
7	VSS		
8	VSS		
9	TEST1	Test Pin (OPEN)	3)
10	TEST2	Test Pin (OPEN)	3)
11	VSS	GND (0V)	1)
12	RX0-	Pixel Data	2)
13	RX0+		
14	VSS	GND (0V)	1)
15	RX1-	Pixel Data	2)
16	RX1+		
17	VSS	GND (0V)	1)
18	RX2-	Pixel Data	
19	RX2+		
20	VSS	GND (0V)	1)
21	CLK-	Pixel Clock	2)
22	CLK+		
23	VSS	GND (0V)	1)
24	RX3-	Pixel Data	2)
25	RX3+		
26	VSS	GND (0V)	1)
27	AMODE	LVDS Mode Select	5)
28	TEST3	Test Pin (OPEN)	3)
29	TEST4	Test Pin (OPEN)	3)
30	VSS	GND (0V)	1)

Notes 1) All Vss pins should be grounded.
2) RXn- and RXn+ (n=0,1,2,3), CLK- and CLK+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.
3) Please keep open. HITACHI test only.
4) All V_{DD} pins should be connected to +5.0 V (typ.).
5) Please refer to page 9-4/6 "LVDS interface" for LVDS data mapping.
6) Pin assignment is as follows.



(Figure from top-view)

5.2 BACK-LIGHT UNIT

CN2 : TARNG YU Enterprise: TU2001WNR-12S or Equivalent
(Matching connector : JST: PHR-12 or TARNG YU Enterprise: TU2001HNO-12)

Pin No.	Symbol	Description	Note
1	V_{IN}	Power Supply (typ. 12.0V	1)
2	V_{IN}		
3	V_{IN}		
4	V_{IN}		
5	ON/OFF	High : Backlight ON, Low : Backlight OFF	4)
6	V_{SS}	GND (0V)	2)
7	V_{SS}		
8	V_{BC}	Brightness Control Signal	5),6)
9	PWM	PWM Dimming Signal	3),6)
10	FLT	LED Fault Signal	7)
11	V_{SS}	GND (0V)	2)
12	V_{SS}		

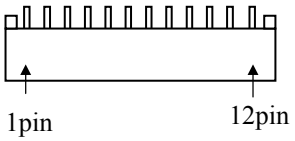
Notes

1) V_{IN} pins should be connected to +12.0V (Typ.).
2) V_{SS} pins should be grounded. The metal bezel is internally connected to GND.
3) High level:2.5 ~ 5.0V, Low level:0 ~ 0.8V
4) High level:2.5 ~ 5.0V, Low level:0 ~ 0.8V
5) Input Voltage : 1.0 ~ 3.6V DC (Brightness becomes maximum at 3.3 +/- 0.3V.)
6) These signals should not be inputted simultaneously. i.e.
when the PWM signal is to be inputted, please set the terminal of V_{BC} to NC. Or
when the V_{BC} signal is to be inputted, please set the PWM terminal to NC.
7) Depending on the state of the LED string, the following voltage is output.

Voltage Level	Condition	Definition
2.1～3.3V	Normal Operation	—
0～0.8V	LED String Open Circuit	One or more strings are occured open circuit.
	LED String Short Circuit	One or more strings are occured short circuit between string+ and string-.

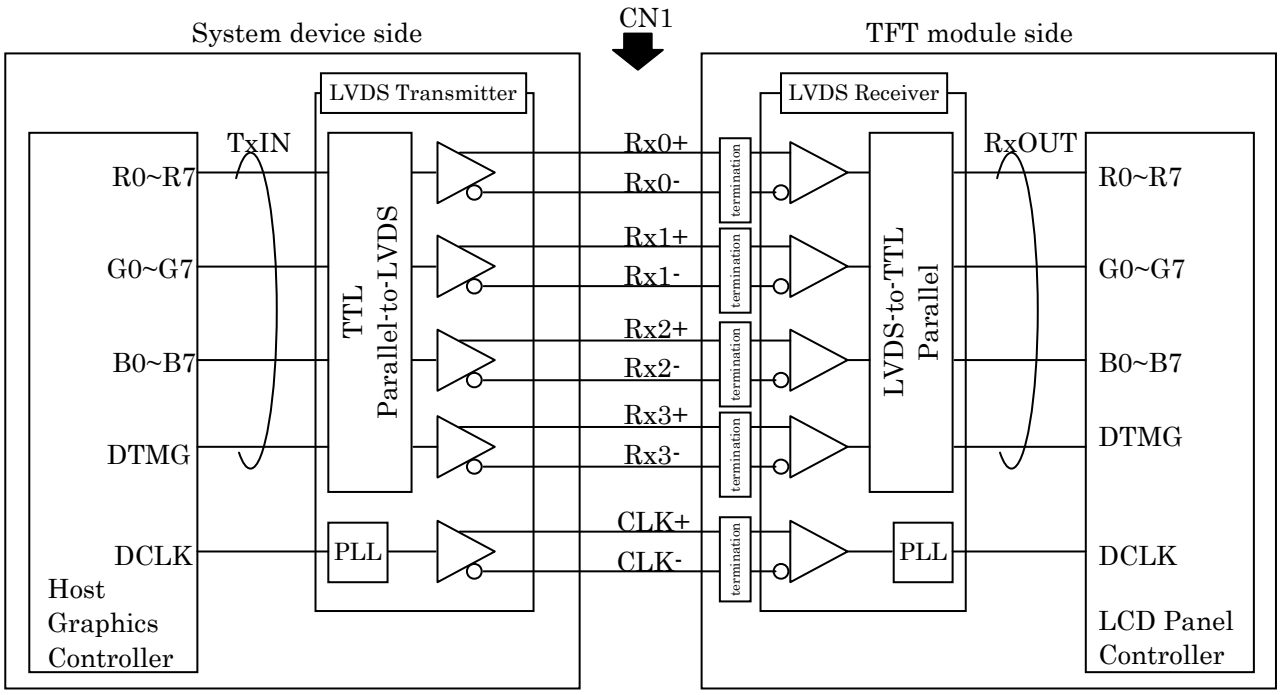
If this is not used in particular, please set the terminal of FLT to NC (No Connection).

8) Pin assignment is as follows.



(Figure from top-view)

BLOCK DIAGRAM OF INTERFACE



Receiver: Equivalent of THC63LVDF84B by THine

R0~7 : R data
G0~7 : G data
B0~7 : B data
DTMG : Display timing data

Notes 1) The system must have a LVDS transmitter to drive a module.
2) The impedance of LVDS cable shall be about 100 ohms per twist-pair line when it is used differentially.

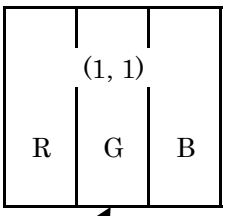
LVDS INTERFACE

27pin AMODE	Signal	Transmitter		Interface Connector		Receiver		TFT Control Input
		Pin	Input	System Device	TFT Module	Pin	Output	
=L (GND)	R0 (LSB)	51	TxIN0	Tx OUT0+	Rx IN0+	27	RxOUT0	R0 (LSB)
	R1	52	TxIN1			29	RxOUT1	R1
	R2	54	TxIN2			30	RxOUT2	R2
	R3	55	TxIN3			32	RxOUT3	R3
	R4	56	TxIN4			33	RxOUT4	R4
	R5	3	TxIN6	Tx OUT0-	Rx IN0-	35	RxOUT6	R5
	G0 (LSB)	4	TxIN7			37	RxOUT7	G0 (LSB)
	G1	6	TxIN8	Tx OUT1+	Rx IN1+	38	RxOUT8	G1
	G2	7	TxIN9			39	RxOUT9	G2
	G3	11	TxIN12			43	RxOUT12	G3
	G4	12	TxIN13			45	RxOUT13	G4
	G5	14	TxIN14			46	RxOUT14	G5
	B0 (LSB)	15	TxIN15	Tx OUT1-	Rx IN1-	47	RxOUT15	B0 (LSB)
	B1	19	TxIN18	Tx OUT2+	Rx IN2+	51	RxOUT18	B1
	B2	20	TxIN19			53	RxOUT19	B2
	B3	22	TxIN20			54	RxOUT20	B3
	B4	23	TxIN21			55	RxOUT21	B4
	DCLK	24	TxIN22			1	RxOUT22	B5
	RSVD 1)	27	TxIN24	Tx OUT2-	Rx IN2-	3	RxOUT24	Not use
	RSVD 1)	28	TxIN25			5	RxOUT25	Not use
	DTMG	30	TxIN26			6	RxOUT26	DTMG
	R6	50	TxIN27	Tx OUT3+	Rx IN3+	7	RxOUT27	R6
	R7 (MSB)	2	TxIN5			34	RxOUT5	R7 (MSB)
	G6	8	TxIN10			41	RxOUT10	G6
	G7 (MSB)	10	TxIN11			42	RxOUT11	G7 (MSB)
	B6	16	TxIN16			49	RxOUT16	B6
	B7 (MSB)	18	TxIN17	Tx OUT3-	Rx IN3-	50	RxOUT17	B7 (MSB)
	RSVD 1)	25	TxIN23			2	RxOUT23	Not use
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

27pin AMODE	Signal	Transmitter		Interface Connector		Receiver		TFT Control Input
		Pin	Input	System Device	TFT Module	Pin	Output	
=H (3.3V)	R2	51	TxIN0	Tx OUT0+	Rx IN0+	27	RxOUT0	R2
	R3	52	TxIN1			29	RxOUT1	R3
	R4	54	TxIN2			30	RxOUT2	R4
	R5	55	TxIN3			32	RxOUT3	R5
	R6	56	TxIN4			33	RxOUT4	R6
	R7 (MSB)	3	TxIN6	Tx OUT0-	Rx IN0-	35	RxOUT6	R7 (MSB)
	G2	4	TxIN7	Tx OUT1+	Rx IN1+	37	RxOUT7	G2
	G3	6	TxIN8			38	RxOUT8	G3
	G4	7	TxIN9			39	RxOUT9	G4
	G5	11	TxIN12			43	RxOUT12	G5
	G6	12	TxIN13			45	RxOUT13	G6
	G7 (MSB)	14	TxIN14			46	RxOUT14	G7 (MSB)
	B2	15	TxIN15	Tx OUT1-	Rx IN1-	47	RxOUT15	B2
	B3	19	TxIN18	Tx OUT2+	Rx IN2+	51	RxOUT18	B3
	B4	20	TxIN19			53	RxOUT19	B4
	B5	22	TxIN20			54	RxOUT20	B5
	B6	23	TxIN21			55	RxOUT21	B6
	B7 (MSB)	24	TxIN22			1	RxOUT22	B7 (MSB)
	RSVD 1)	27	TxIN24	Tx OUT2-	Rx IN2-	3	RxOUT24	Not use
	RSVD 1)	28	TxIN25			5	RxOUT25	Not use
	DTMG	30	TxIN26			6	RxOUT26	DTMG
	R0 (LSB)	50	TxIN27	Tx OUT3+	Rx IN3+	7	RxOUT27	R0 (LSB)
	R1	2	TxIN5			34	RxOUT5	R1
	G0 (LSB)	8	TxIN10			41	RxOUT10	G0 (LSB)
	G1	10	TxIN11			42	RxOUT11	G1
	B0 (LSB)	16	TxIN16			49	RxOUT16	B0 (LSB)
	B1	18	TxIN17	Tx OUT3-	Rx IN3-	50	RxOUT17	B1
	RSVD 1)	25	TxIN23			2	RxOUT23	Not use
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

Note 1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

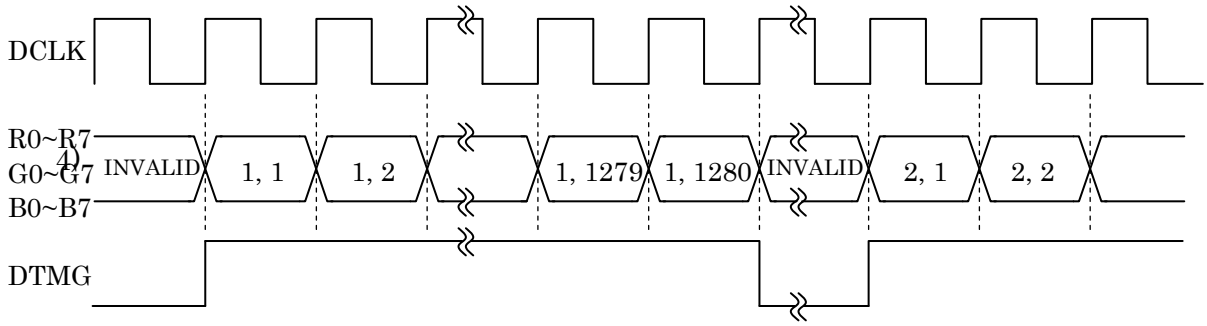
CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE



R0~R7 : R data
G0~G7 : G data
B0~B7 : B data

1, 1	1, 2	1, 3	- - - - - - - - - - - - - - -	1, 1280
2, 1	2, 2	2, 3	- - - - - - - - - - - - - - -	2, 1280
3, 1	3, 2	3, 3	- - - - - - - - - - - - - - -	3, 1280
⋮	⋮	⋮		⋮
768, 1	768, 2	768, 3	- - - - - - - - - - - - - - -	768, 1280

4)



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color \ Input data		R data								G data								B data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

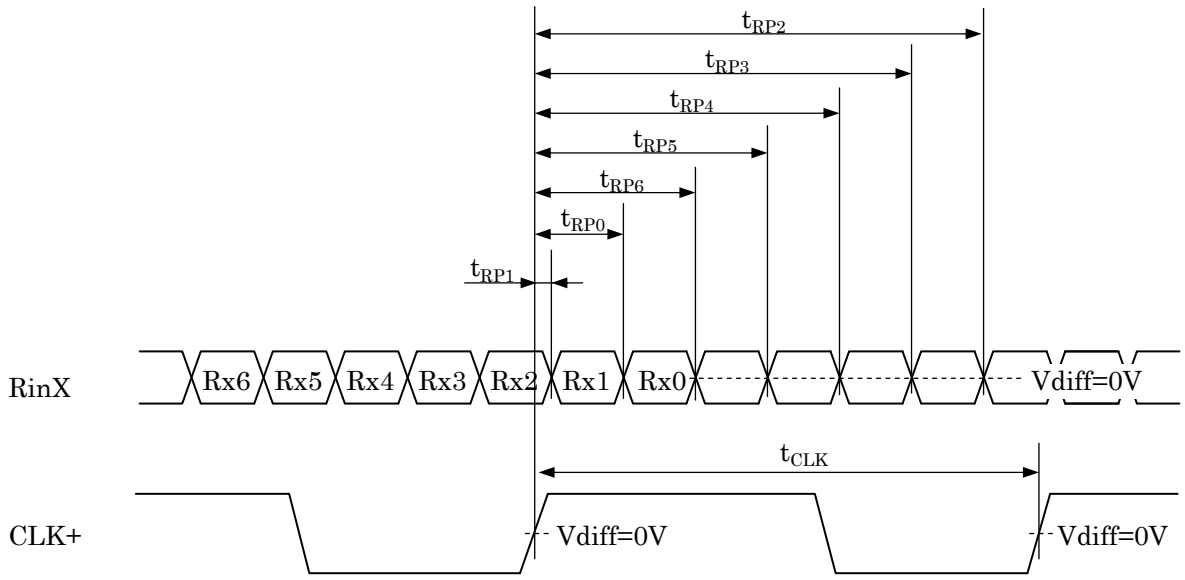
Notes 1) Definition of gray scale: Color (n)

n indicates gray scale level. Higher n means brighter level.

2) Data signals: 1: High, 0: Low

6. TIMING DIAGRAMS OF INTERFACE TIMING

6.1 LVDS RECEIVER TIMING
(Interface of TFT module)

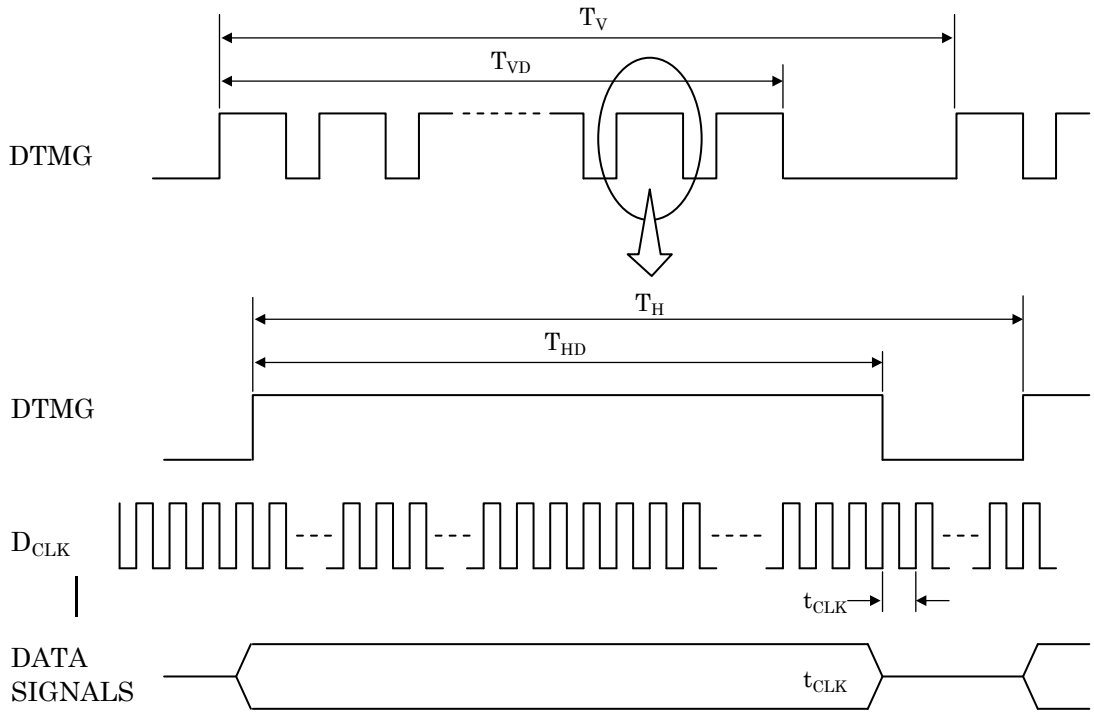


RinX=(RinX+) - (RinX-) (X=0,1,2)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	$1/t_{CLK}$	65	66	73	MHz	
RinX (X=0,1,2)	0 data position	t_{RP0}	$1/7t_{CLK}$-0.29	$1/7t_{CLK}$	$1/7t_{CLK}$+0.29	ns	
	1st data position	t_{RP1}	-0.29	0	+0.29		
	2nd data position	t_{RP2}	$6/7t_{CLK}$-0.29	$6/7t_{CLK}$	$6/7t_{CLK}$+0.29		
	3rd data position	t_{RP3}	$5/7t_{CLK}$-0.29	$5/7t_{CLK}$	$5/7t_{CLK}$+0.29		
	4th data position	t_{RP4}	$4/7t_{CLK}$-0.29	$4/7t_{CLK}$	$4/7t_{CLK}$+0.29		
	5th data position	t_{RP5}	$3/7t_{CLK}$-0.29	$3/7t_{CLK}$	$3/7t_{CLK}$+0.29		
	6th data position	t_{RP6}	$2/7t_{CLK}$-0.29	$2/7t_{CLK}$	$2/7t_{CLK}$+0.29		

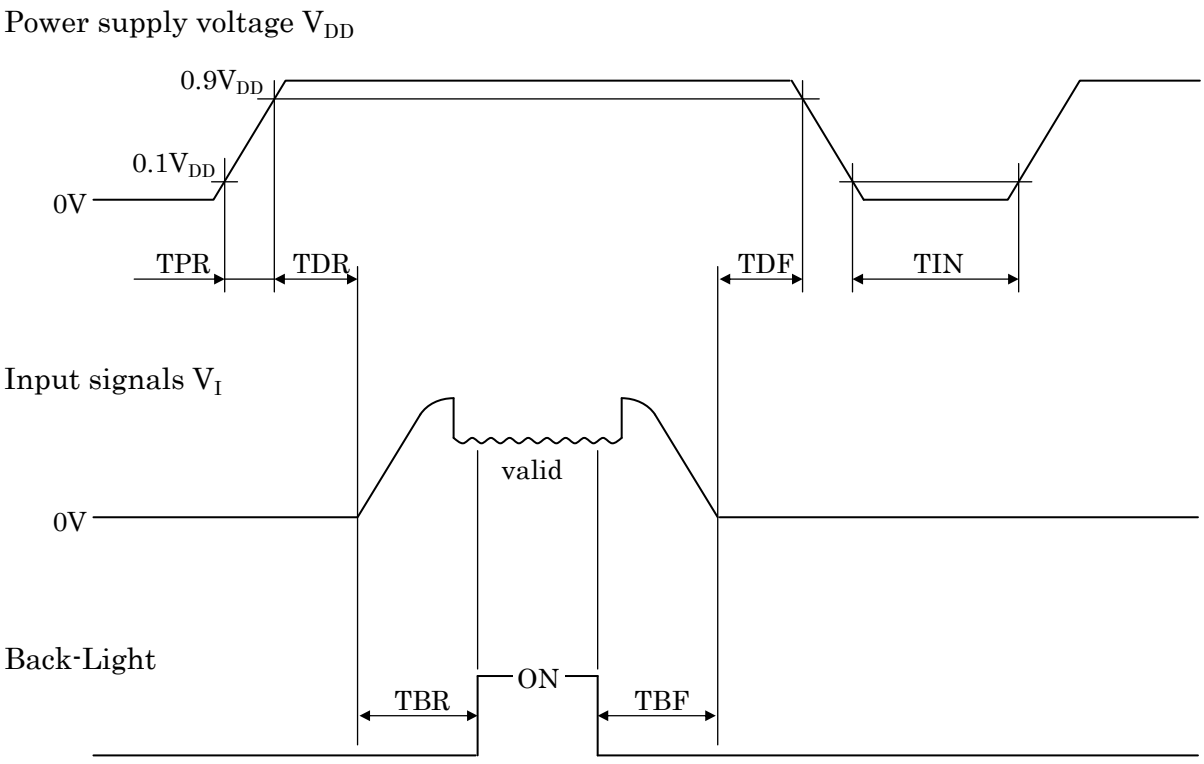
6.2 TIMING CONVERTER TIMING

(Input timing for transmitter)



Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Cycle time	t_{CLK}	13.7	15.1	15.4	ns	
	Duty	D	0.35	0.5	0.65	-	
DTMG	Horizontal period	T_H	1396	1406	1450	t_{CLK}	
	Horizontal width-Active	T_{HD}	1280	1280	1280	t_{CLK}	
	Vertical period	T_V	773	783	825	T_H	
	Vertical width-Active	T_{VD}	768	768	768	T_H	
	Frame frequency	f_V	55	60	65	Hz	

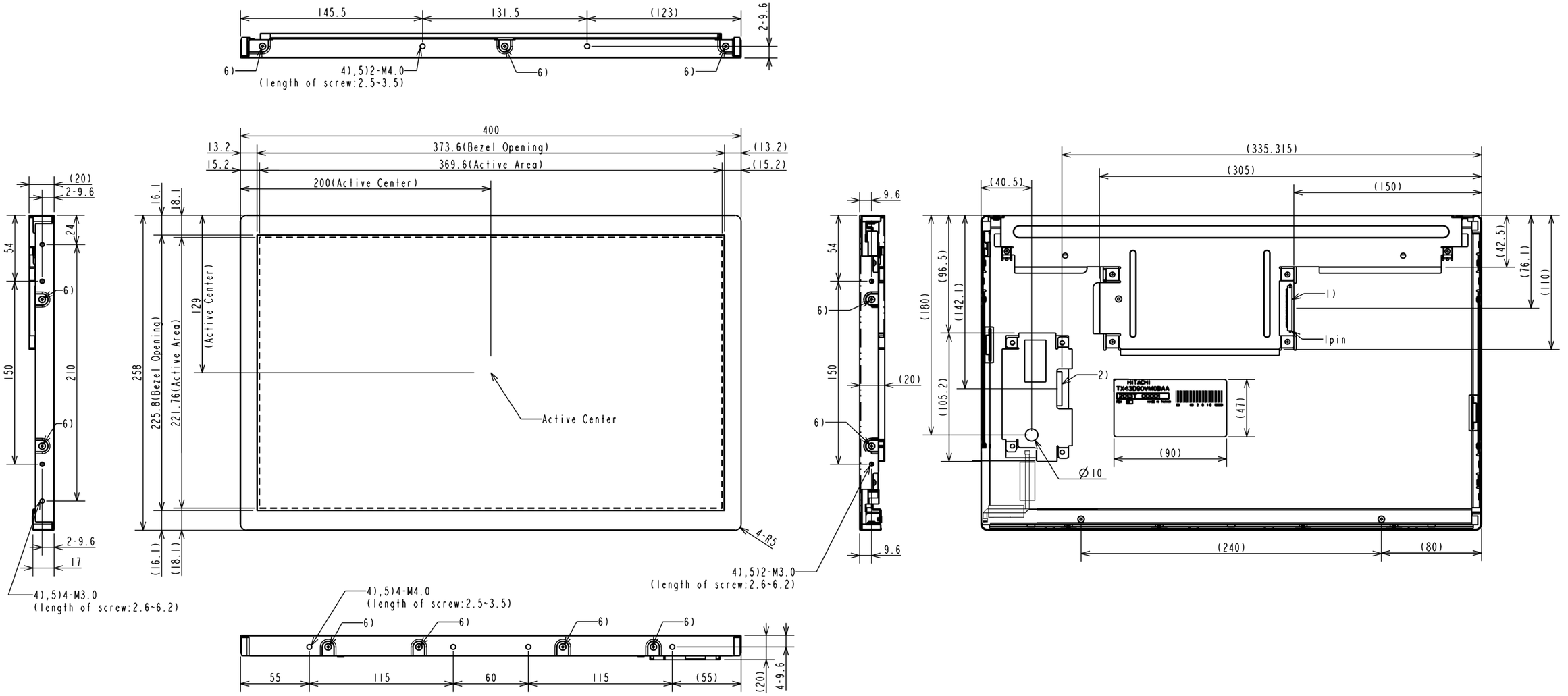
6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

1ms	≤	TPR	≤	10ms
40ms	≤	TDR		
20ms	≤	TDF	≤	50ms
		TIN	≥	1s
		TBR	≥	500ms
		TBF	≥	100ms

7. DIMENSIONAL OUTLINE



Note 1) Interface connector (CN1)
JAE: FI-X30SSLA-HF or equivalent

2) Converter PCB connector (CN2)
TARNG YU Enterprise: TU2001WNR-12S or equivalent

3) Dimension in parentheses are reference value.
The unspecified tolerance: ±0.5mm

4) Hole in mouting panel: M3: 6 holes (right and left side), M4: 6 holes (upper and lower side)

5) Maximum torque for the screw in mounting panel : 0.294N・m (3kgf・cm)

6) There are all screws attached to side of the module.

Unit: mm
Scale:NTS

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