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TENTATIVE

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____ DATE: Aug. 21st ,2012

TECHNICAL DATA

TX18D45VM2BAA

Contents

PROPOSED BY:

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 7.0” WVGA of 16:9 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX18D45VM2BAA
Module Dimensions	165.0(W) mm x 106.0(H) mm x 8.0 (D) mm typ.
LCD Active Area	152.4(W) mm x 91.44(H) mm
Pixel Pitch	0.1905(W) mm x 0.1905 (H) mm
Resolution	800 x 3(RGB)(W) x 480(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally White
Display Type	Active Matrix
Number of Colors	262k Colors
Backlight	27 LEDs (3 series x 9)
Weight	126 g
Interface	LVDS 20 pins
Power Supply Voltage	3.3V for LCD; 9.8V for backlight.
Power Consumption	0.80W for LCD; 1.76W for backlight.
Viewing Direction	12 O’clock (without image inversion and least brightness change) 6 O’clock (contrast peak located at)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	0	7.0	V	-
Input Voltage of Logic	VI	-0.3	VDD+0.3	V	Note 1
Operating Temperature	Top	-30	80	°C	Note 2
Storage Temperature	Tst	-30	80	°C	Note 2

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the temperature on the panel surface which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

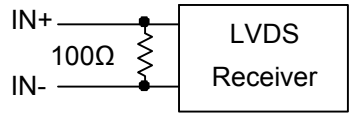
$T_a = 25\ ^{\circ}C,\ \mathrm{VSS} = 0\mathrm{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	VDD	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	VI	VIH	-	-	+100	mV	Note 1
		VIL	-100	-	-		
Power Supply Current	IDD	VDD-VSS =3.3V	-	243	-	mA	Note 2,3
Vsync Frequency	f_v	-	-	60	66	Hz	Note 4
Hsync Frequency	f_H	-	-	31.2	-	KHz	
DCLK Frequency	f_{CLK}	-	-	32.32	-	MHz	

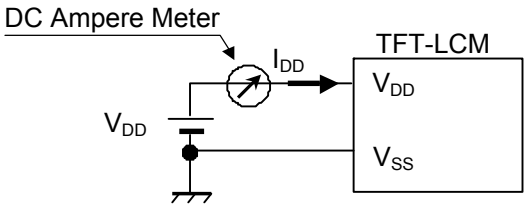
Note 1: VCM=+1.2V

VCM is common mode voltage of LVDS transmitter/receiver.

The input terminal of LVDS transmitter is terminated with 100Ω.



Note 2: An all black check pattern is used when measuring IDD, f_v is set to 60Hz.



Note 3: 1.0A fuse is applied in the module for IDD. For display activation and protection purpose, power supply is recommended larger than 2.5A to start the display and break fuse once any short circuit occurred.

Note 4: For LVDS transmitter input.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	VLED	Backlight Unit	-	9.8	-	V	Note 1
LED Forward Current	ILED	Backlight Unit	-	180	-	mA	-
LED Lifetime	-	180 mA	-	40K	-	hrs	Note 2,3

Note 1: Fig. 5.1 shows the LED backlight circuit. The circuit has 27 LEDs in total.

Note 2: The estimated lifetime is specified as the time to reduce 50% brightness by applying 180 mA at 25°C.

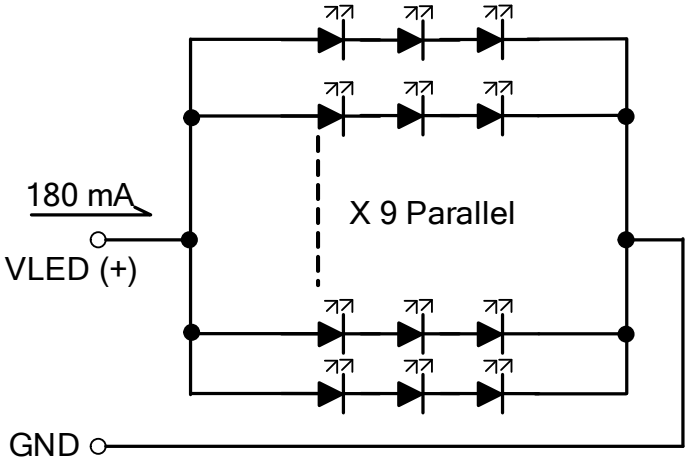


Fig 5.1

Note 3: By applying different ILED, the estimated brightness and LED life time curves are shown as Fig 5.2 and Fig 5.3 for various environment use.

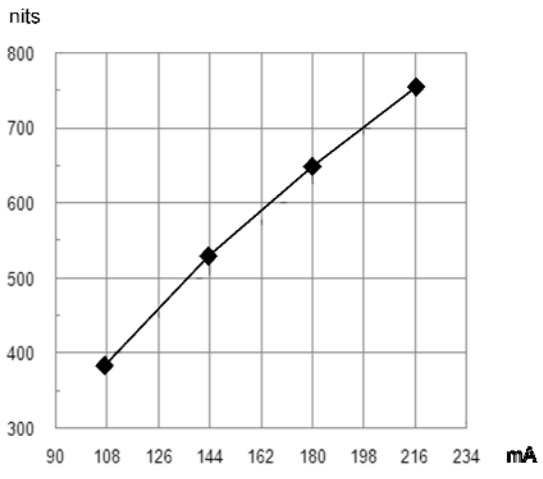


Fig 5.2 LED Current v.s. Brightness

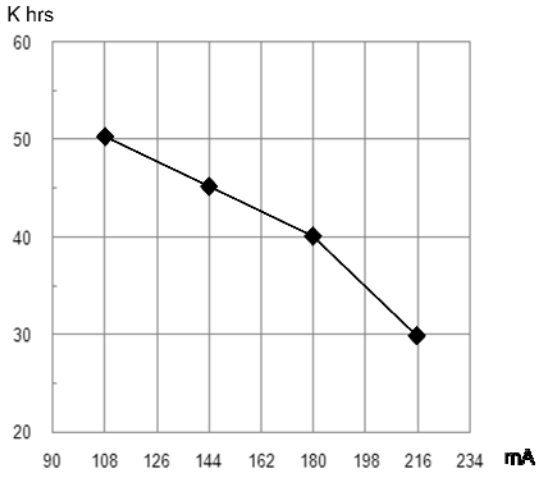


Fig 5.3 LED Current v.s. Lifetime

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room around 500~1000 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C,\ f_v = 60\,\text{Hz}, \text{VDD} = 3.3\text{V}$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	ILED= 180mA	-	600	-	cd/m^2	Note 1
Brightness Uniformity		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	70	-	-	%	Note 2
Contrast Ratio		CR		-	600	-	-	Note 3
Response Time (Rising + Falling)		Tr + Tf	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	20	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	45	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}, \text{CR} \geq 10$	-	70	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}, \text{CR} \geq 10$	-	70	-		
		θ y	$\phi = 90^{\circ}, \text{CR} \geq 10$	-	65	-		
		θ y′	$\phi = 270^{\circ}, \text{CR} \geq 10$	-	65	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	0.56	-	-	Note 6
		Y		-	0.36	-		
	Green	X		-	0.36	-		
		Y		-	0.56	-		
	Blue	X		-	0.16	-		
		Y		-	0.12	-		
	White	X		-	0.31	-		
		Y		-	0.33	-		

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

, which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

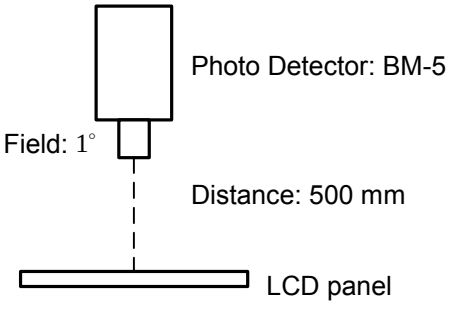


Fig. 6.1

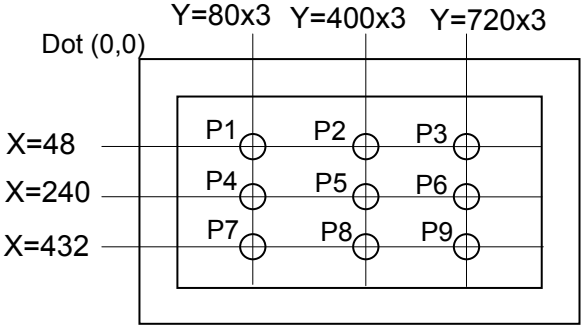


Fig. 6.2

Note 3: The Contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.

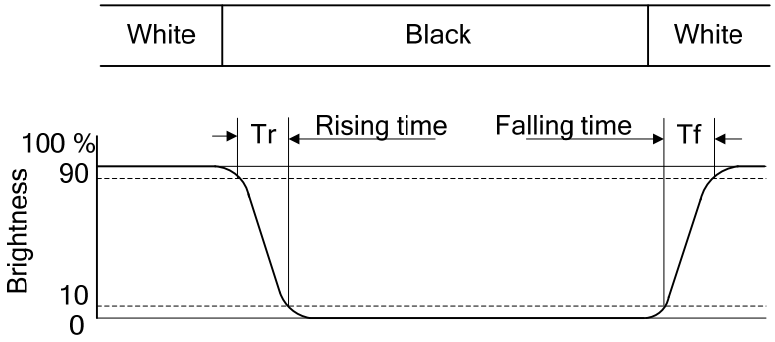


Fig 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The viewing direction of this display is 12 o'clock, which means that a photograph with gray scale would not be reversed in color and the brightness change would be less from this direction. However, the best contrast peak would be located at 6 o'clock.

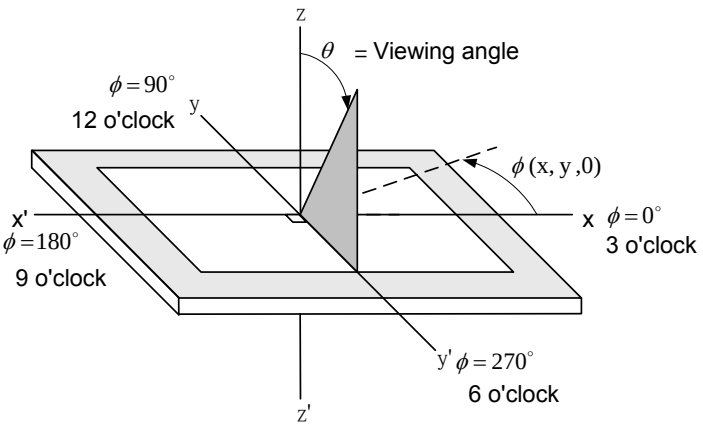
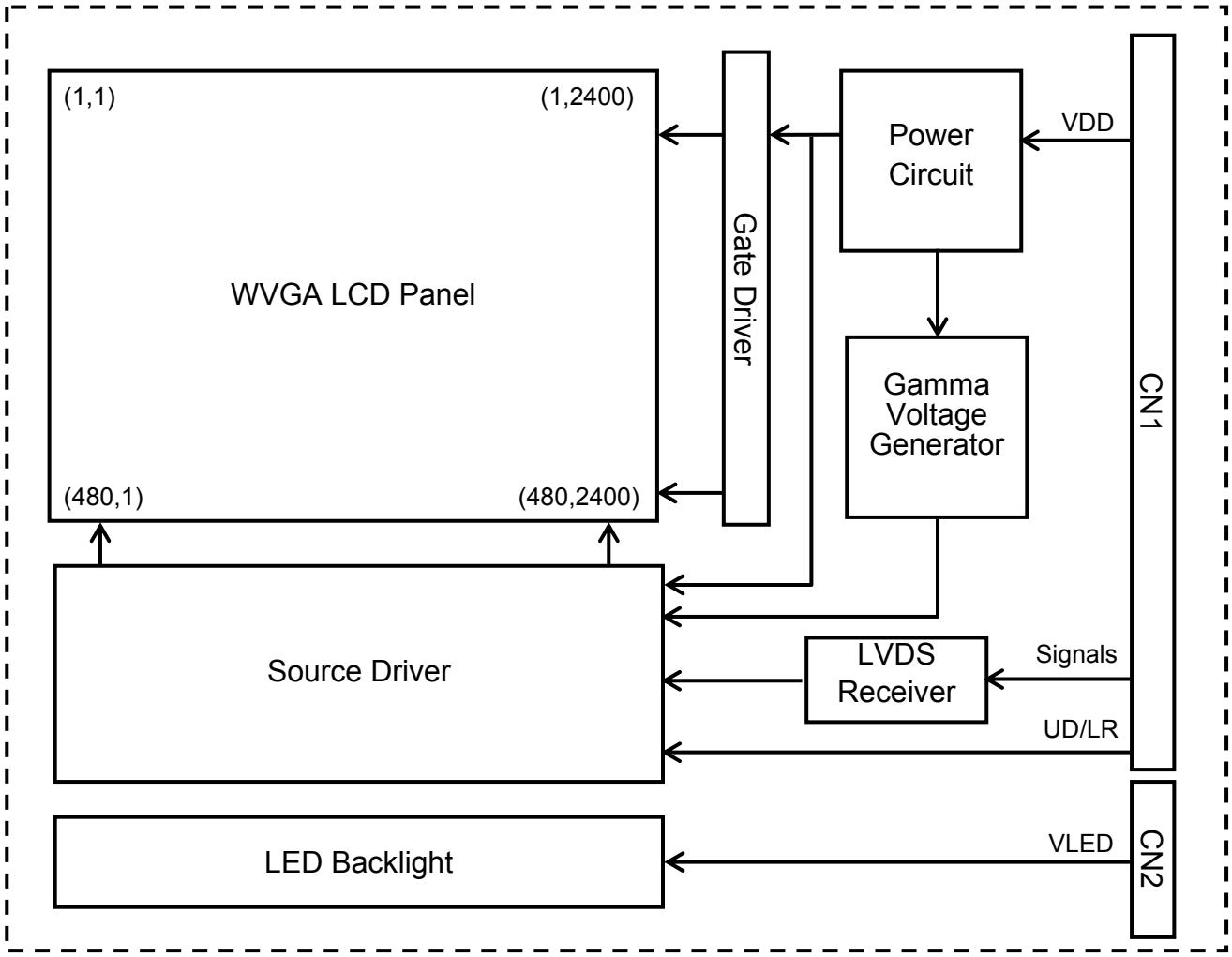


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

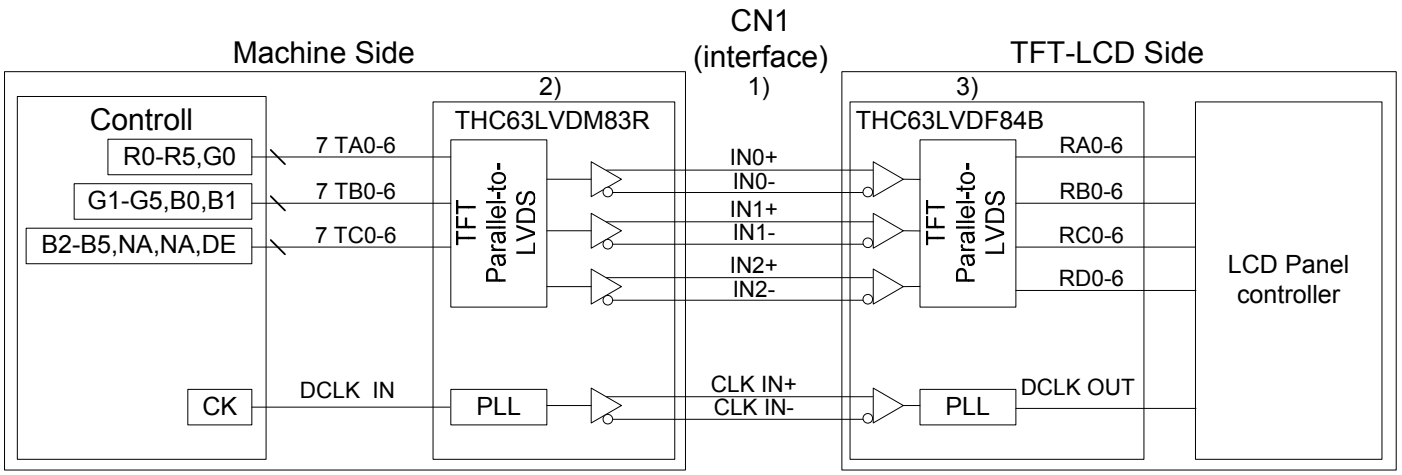
The display interface connector (CN1) is FA5B040HP1R3000 made by JAE, and pin assignment is as below：

Pin No.	Symbol	Signal
1	VDD	Power Supply for Logic
2	LR	H: Left to right (Default); L: Right to Left
3	UD	L: Up to down (Default); H: Down to up
4	Vss	Ground
5	In0-	R0~R5,G0
6	In0+	
7	Vss	Ground
8	In1-	G1~G5, B0~B1
9	In1+	
10	Vss	Ground
11	In2-	B2~B5,DE
12	In2+	
13	Vss	Ground
14	CLK In-	Pixel clock
15	CLK In+	
16	Vss	Ground
17	NC	No Connection
18	NC	No Connection
19	NC	No Connection
20	NC	No Connection

The backlight connector (CN2) is BHR-03VS-1 made by JAE, and pin assignment of backlight is as below：

Pin No.	Signal	Level	Function
1	VLED+	-	Power Supply for LED
2	NC	-	No connection
3	VLED-	-	GND

8.2 LVDS INTERFACE

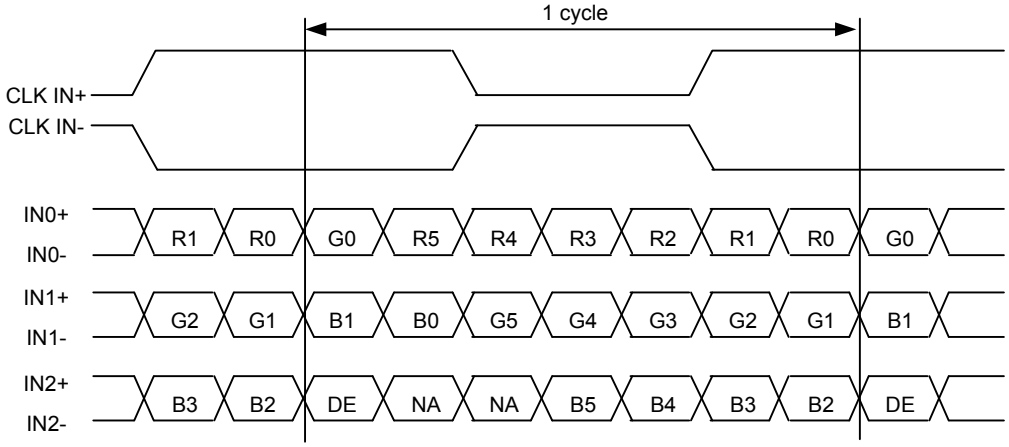


Note 1: LVDS cable impedance should be 100 ohms per signal line when each 2-lines (+, -) is used in differential mode.

Note 2: The recommended transmitter, THC63LVDM83R, is made by Thine or equivalent, which is not contained in the module.

Note 3: The receiver built-in the module is THC63LVDF84B made by Thine.

8.3 LVDS DATA FORMAT



DE: Display Enable

NA: Not Available

8.4 INTERFACE TIMING SPECIFICATIONS

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (Vsync) = 60 Hz to define. If 60 Hz is not the aim to set, less than 66 Hz for Vsync is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Cycle frequency	$1/t_{CLK}$	-	32.32	-	MHz
	Duty	D	-	0.5	-	-
DE	Set up time	t_{SI}	6	-	-	ns
	Hold time	t_{HI}	6	-	-	
	Horizontal cycle	t_H	-	1036	-	t_{CLK}
	Horizontal valid data width	t_{HD}	-	800	-	
	Horizontal porch width	t_{HB}	-	236	-	
	Vertical cycle	tv	-	520	-	t_H
	Vertical valid data width	t_{VD}	-	480	-	
	Vertical porch width	t_{VB}	-	40	-	
Data	Set up time	t_{SD}	6	-	-	ns
	Hold time	t_{HD}	6	-	-	

8.5 TIMING CHART

DE (Data Enable) is the signal to determine valid data , and the timing of DE can be determined from Hsync and the Vsync as below. For this display, only DE and DCLK are the essential signals. Hsync and Vsync are not necessary to connect to display interface after DE has been generated and input.

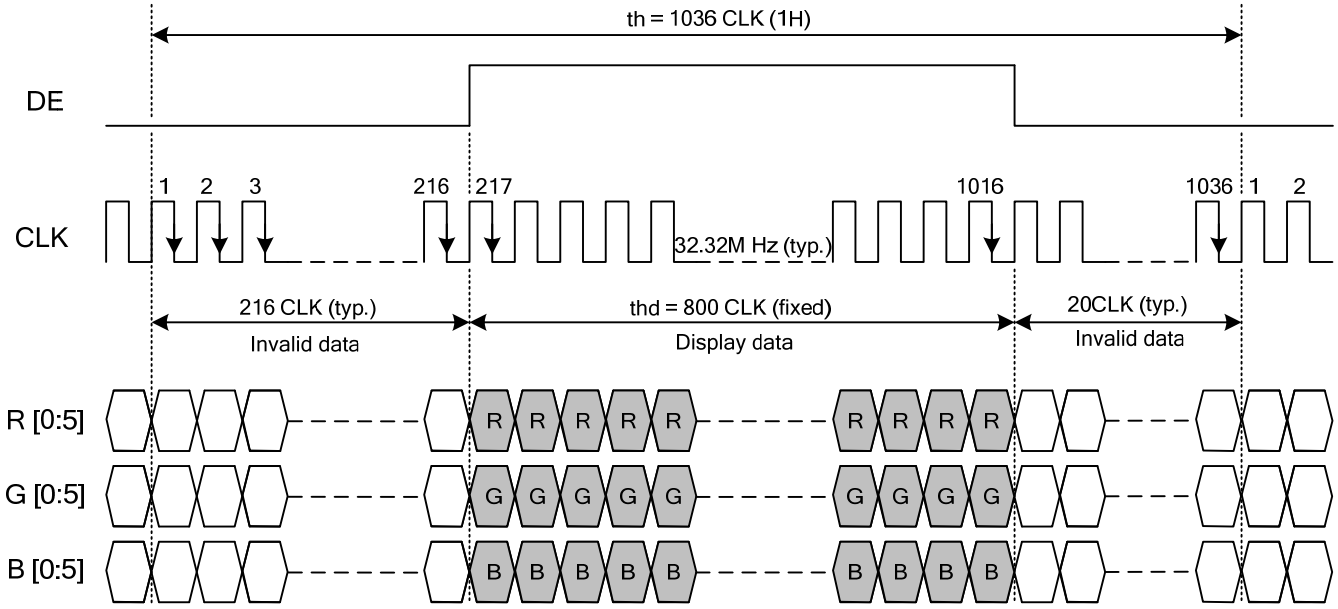


Fig. 9.3 Horizontal Timing of DE Mode

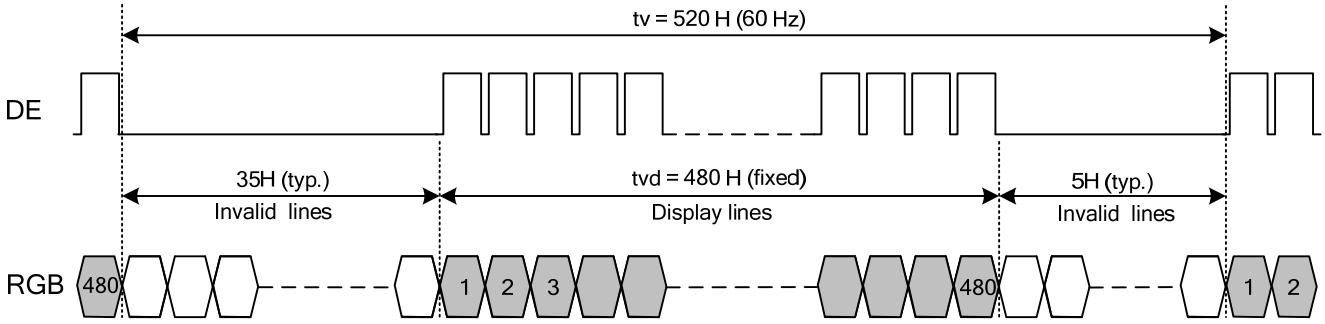


Fig. 9.4 Vertical Timing of DE Mode

CLOCK AND DATA INPUT TIMING

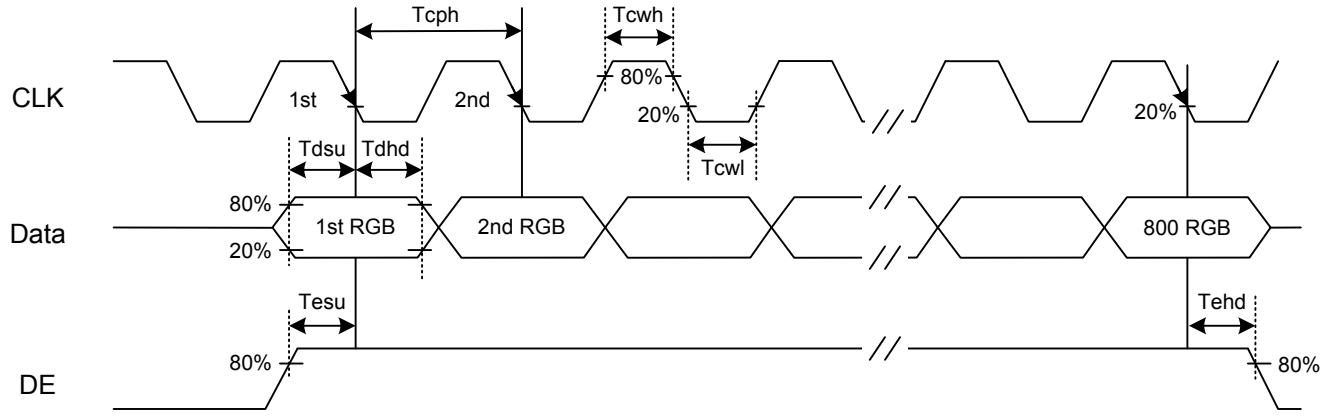
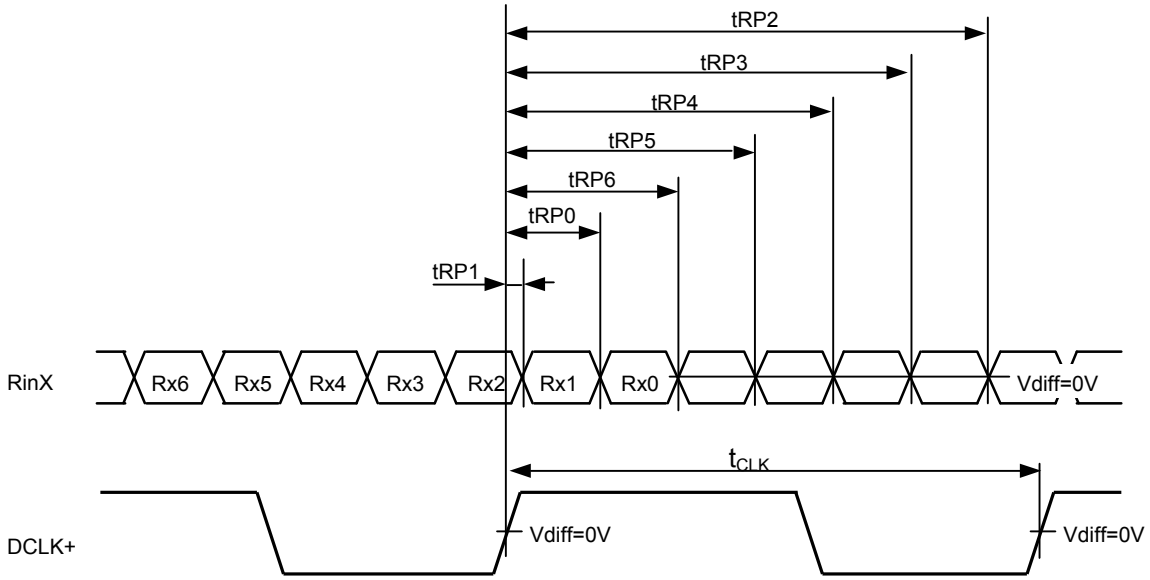


Fig. 9.5 Setup & Hold Time of Data and DE signal.

8.6 LVDS RECEIVER TIMING



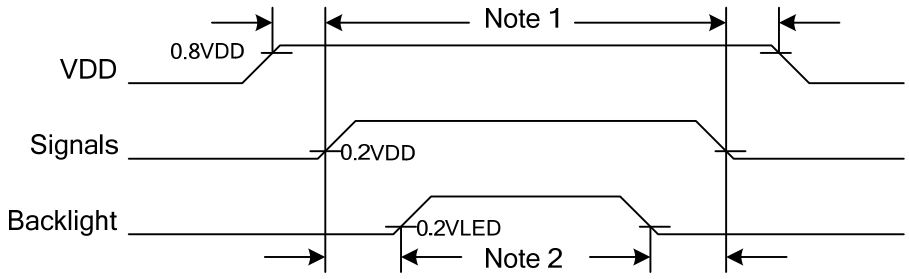
RinX= (RinX+)-(RinX-) (X=0, 1, 2)

Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Frequency	1/ t_{CLK}	-	32.32	-	MHz
RinX (X=0,1,2)	0 data position	tRP0	1/7* t_{CLK} -0.49	1/7* t_{CLK}	1/7* t_{CLK} +0.49	ns
	1st data position	tRP1	-0.49	0	+0.49	
	2nd data position	tRP2	6/7* t_{CLK} -0.49	6/7* t_{CLK}	6/7* t_{CLK} +0.49	
	3rd data position	tRP3	5/7* t_{CLK} -0.49	5/7* t_{CLK}	5/7* t_{CLK} +0.49	
	4th data position	tRP4	4/7* t_{CLK} -0.49	4/7* t_{CLK}	4/7* t_{CLK} +0.49	
	5th data position	tRP5	3/7* t_{CLK} -0.49	3/7* t_{CLK}	3/7* t_{CLK} +0.49	
	6th data position	tRP6	2/7* t_{CLK} -0.49	2/7* t_{CLK}	2/7* t_{CLK} +0.49	

8.7 DATA INPUT for DISPLAY COLOR

	COLOR & Gray Scale	Data Signal																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

8.8 POWER SEQUENCE



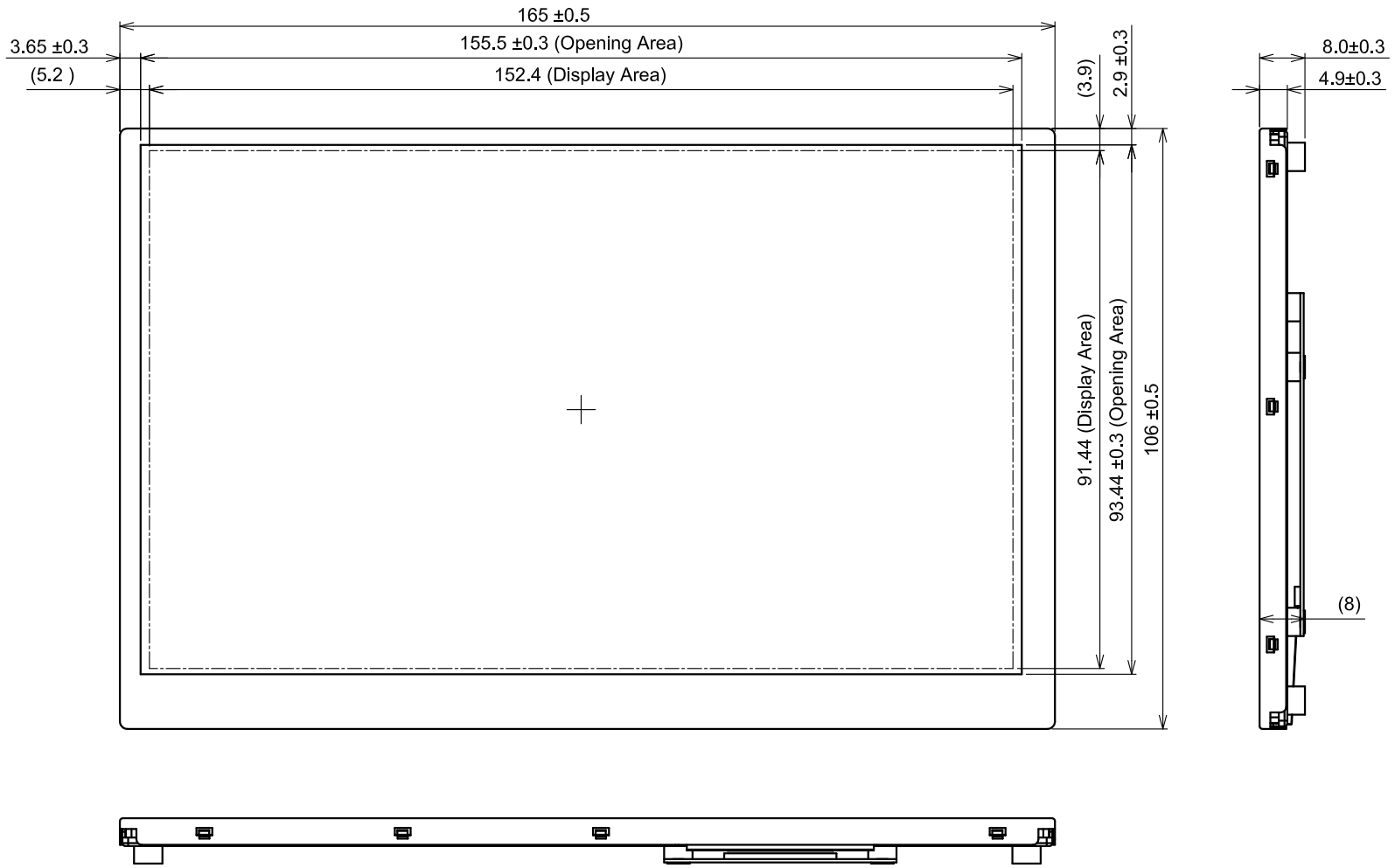
Power Sequence Timing

Note 1: In order to avoid any damages, VDD has to be applied before all other signals. The opposite is true for power off where VDD has to be remained on until all other signals have been switch off. The recommended time period is 1 second. Hot plugging might cause display damage due to incorrect power sequence, please pay attention on interface connecting before power on.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

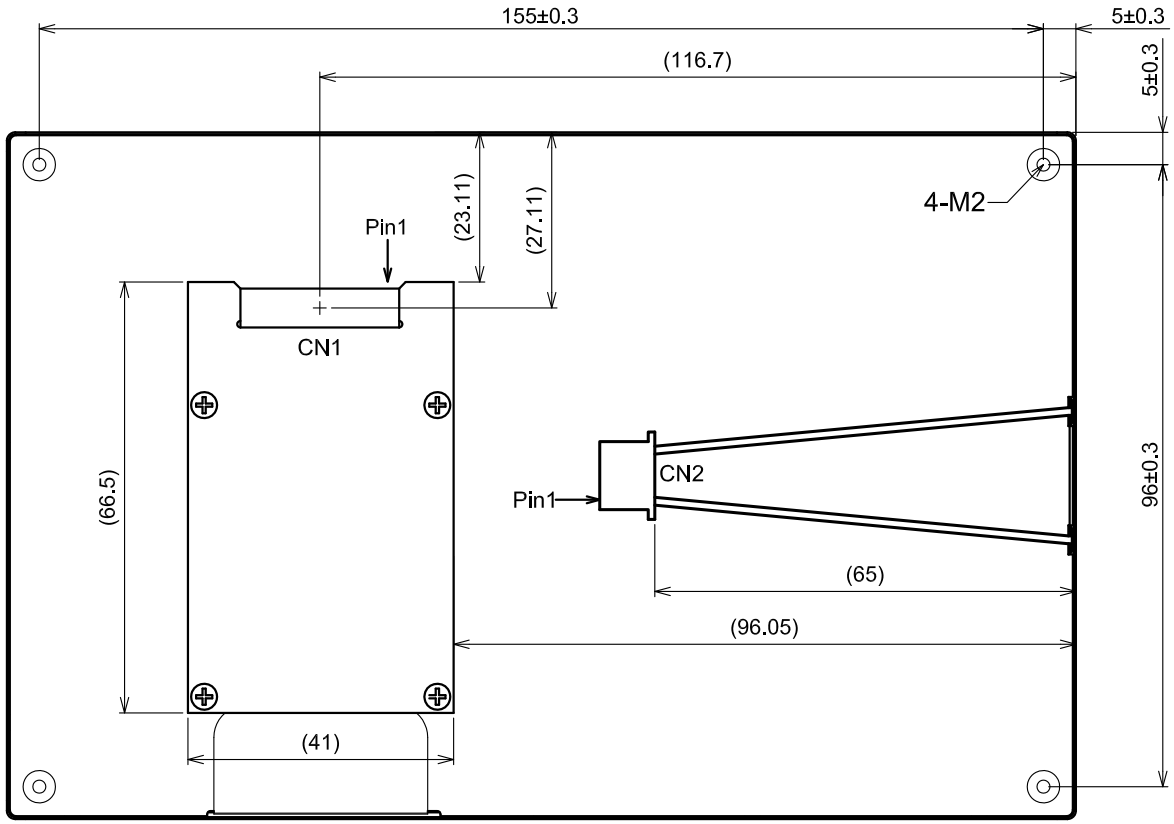
9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



Scale : NTS
Unit : mm

9.2 REAR VIEW



Scale : NTS
Unit : mm

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