PRELIMINARY

NLT Technologies, Ltd.

TFT COLOR LCD MODULE

NL128102AC29-17

48cm (19.0 Type)
SXGA
LVDS interface (2port)

PRELIMINARY DATA SHEET

DOD-PP-1707 (5th edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PP-1694(4)

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INTRODUCTION

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Examples: Office equipment, audio and visual equipment, communication equipment, test and measurement equipment, personal electronic equipment, home electronic appliances, car navigation system (with no vehicle control functions), seat entertainment monitor for vehicles and airplanes, fish finder (except marine radar integrated type), PDA, etc.

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Examples: Vehicle/train/ship control system, traffic signals system, traffic information control system, air traffic control system, surgery/operation equipment monitor, disaster/crime prevention system, etc.

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Examples: Aerospace system (except seat entertainment monitor), nuclear control system, life support system, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL128102AC29-17 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Color monitor system

1.3 FEATURES

- Ultra-wide viewing angle (Super Fine TFT (SFT))
- Wide color gamut
- High luminance
- High contrast
- LVDS interface
- Selectable LVDS data input map
- LED backlight type
- LED driver circuit Built-in

2. GENERAL SPECIFICATIONS

Display area	376.32 (H) × 301.056 (V) mm
Diagonal size of display	48cm (19.0 inches)
Drive system	a-Si TFT active matrix
Display color	16,777,216 colors
Pixel	1,280 (H) × 1,024 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.098 (H) × 0.294 (V) mm
Pixel pitch	0.294 (H) × 0.294 (V) mm
Module size	396.0 (W) (typ.) × 324.0 (H) (typ.) × 18.0 (D) (typ.) mm
Weight	2,100 (typ.), 2,310 (max.) g
Contrast ratio	1000:1 (typ.)
Viewing angle	*At the contrast ratio ≥10:1* • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)
Designed viewing direction	• Viewing angle with optimum grayscale (γ≒ 2.2): Normal axis (perpendicular)
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5600]
Color gamut	*At LCD panel center* 72% (typ.) [against NTSC color space]
Response time	*Ton+Toff (10%←→ 90%)* 25ms (typ.)
Luminance	*At the maximum luminance control* 800 cd/m^2 (typ.)
Signal system	LVDS 2port (Receiver: THC63LVDF84B, THine Electronics Inc. or equivalent) [8bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)]
Power supply voltage	LCD panel signal processing board: 5.0V LED Driver board: 12.0V
Backlight	LED backlight type built in LED Driver Circuit
Power consumption	*At BL Duty Ratio=100%, Checkered flag pattern* 45.0W (typ.) include LED driver board

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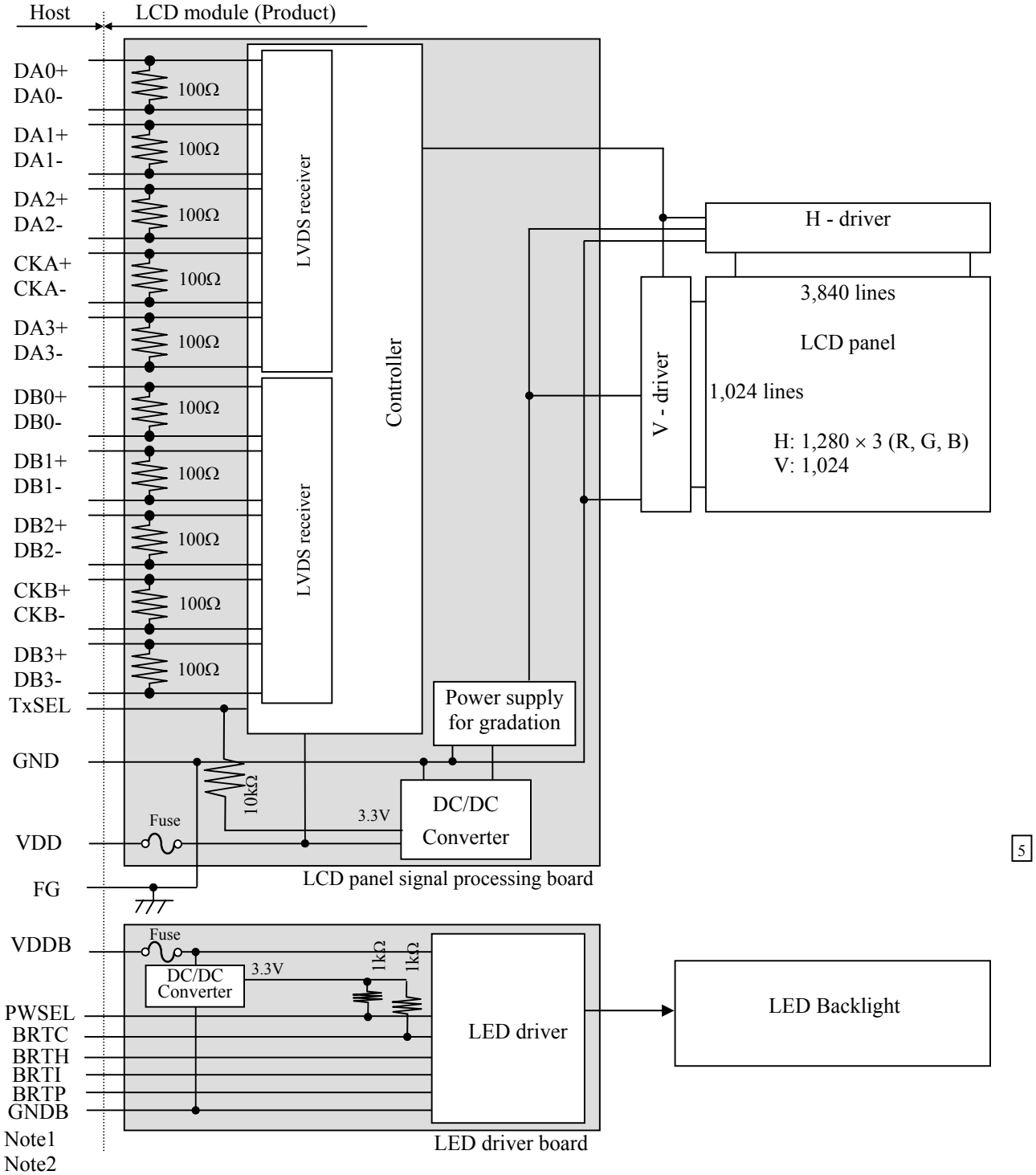
3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), GNDB (LED driver ground) and FG (Frame ground) in the LCD module are as follow.

GND - FG	Connected
GND - GNDB	NOT connected
FG - GNDB	NOT connected

Note2: GND, GNDB and FG must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	396.0 ± 0.5 (W) × 324.0 ± 0.5 (H) × 18.0± 0.5 (D) (typ.)	Note1 Note2	mm
Display area	376.32 (H) × 301.056 (V)	Note1	mm
Weight	2,100 (typ.), 2,310 (max.)		g

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Note1: Excluding a bulge of the cover for the signal processing board and the LED driver board.
Note2: See "**8. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +6.5	V	Ta = 25°C
	LED driver		VDDB	-0.3 to +25.0		
Input voltage for signals	Display signals Note1		VD	-0.3 to +2.4	V	
	Function signals Note2		VF	-0.3 to +3.3		
	Function signal for LED driver		BRTC	-0.3 to +6.3		
			BRTI	-0.3 to +6.0		
			BRTP	-0.3 to +5.5		
			PWSEL	-0.3 to +6.5		
Storage temperature			Tst	-30 to +80	°C	-
Operating temperature		Front surface	TopF	-20 to +70	°C	Note3
		Rear surface	TopR	-20 to +70	°C	Note4
Relative humidity Note5			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 55	%	50°C < Ta ≤ 60°C
				≤ 36	%	60°C < Ta ≤ 70°C
Absolute humidity Note5			AH	≤ 70 Note6	g/m^3	Ta > 70°C
Operating altitude			-	≤ 5,100	m	-20°C≤ Ta ≤ 70°C
Storage altitude			-	≤ 13,600	m	-30°C≤ Ta ≤ 80°C

Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-
Note2: Function signal is TxSEL.
Note3: Measured at LCD panel surface (including self-heat)
Note4: Measured at LCD module's rear shield surface (including self-heat)
Note5: No condensation
Note6: Water amount at Ta= 70°C and RH= 36%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	4.5	5.0	5.5	V	-
Power supply current		IDD	-	700 Note1	900 Note2	mA	at VDD = 5.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM = 1.2V Note3
	Low	VTL	-100	-	-	mV	
Terminating resistance		RT	-	100	-	Ω	-
Input voltage for TxSEL signal	High	VFH	Keep this pin open.			-	TxSEL Note4
	Low	VFL	-	-	0.9	V	
Input current for TxSEL signal		IFL	-400	-	400	μA	

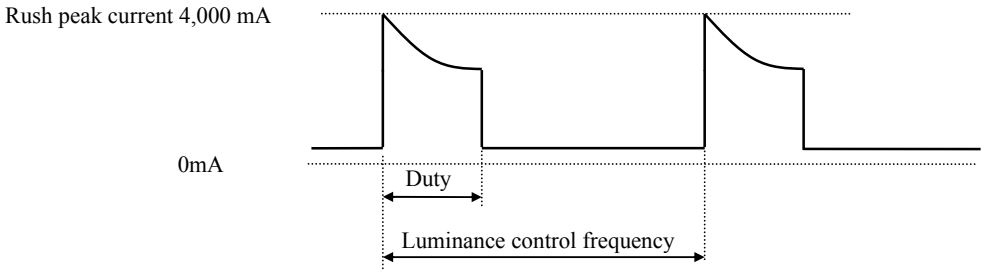
Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS receiver
Note4: TxSEL is pulled-up in the product. (Pull-up resistance: 10kΩ)

4.3.2 LED driver board

(Ta= 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage			VDDB	10.8	12.0	13.2	V	-	
Power supply current			IDDB	-	3,460	4,020	mA	VDDB= 12.0V, At the maximum luminance control	5
Input voltage for signals	BRTI signal		VBI	0.1	-	1.0	V	-	
	BRTP signal	High	VBPH	2.3	-	3.3	V		
		Low	VBPL	0	-	0.6	V		
	BRTC signal	High	VBCH	2.3	-	3.3	V		5
		Low	VBCL	0	-	0.6	V		
	PWSEL signal	High	VBSH	2.3	-	3.3	V		
		Low	VBSL	0	-	0.9	V		
Input current for signals	BRTI signal		IBI	-200	-	200	µA		
	BRTP signal	High	IBPH	-	-	500	µA		
		Low	IBPL	-500	-	-	µA		
	BRTC signal	High	IBCH	-	-	5,000	µA		
		Low	IBCL	-5,000	-	-	µA		
	PWSEL signal	High	IPSH	-	-	5,000	µA		
		Low	IPSL	-5,000	-	-	µA		

4.3.3 LED driver board current wave



Duty:At the maximum luminance control 100% to at the minimum luminance control 1%.
Luminance control frequency: 255 Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000µF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

4.3.4 Power supply voltage ripple

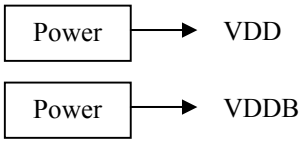
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	5.0V	≤ 100	mVp-p
VDDB	12.0V	≤ 200	mVp-p

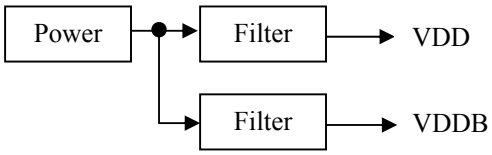
Note1: The permissible ripple voltage includes spike noise.
Note2: The load variation influence does not include.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



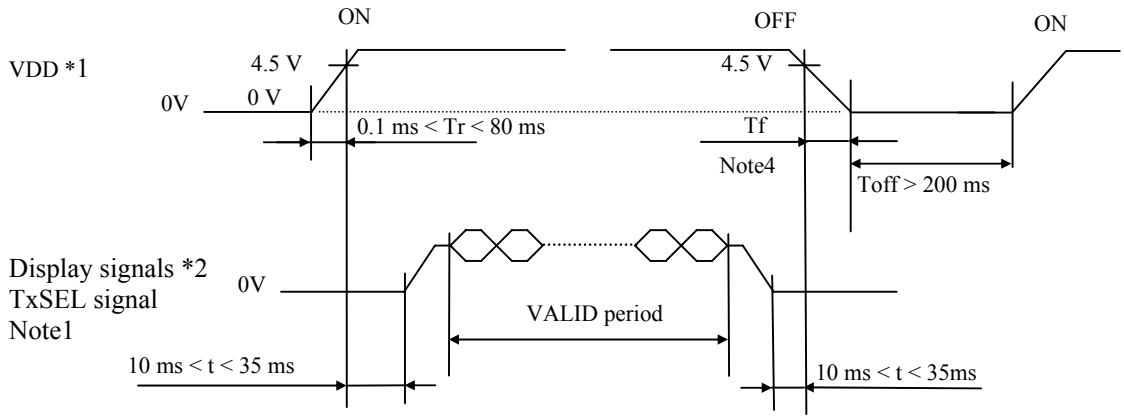
4.3.5 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC32252AD	KAMAYA ELECTRIC Co.,Ltd.	2.5A 32V	6.25A, 5 seconds maximum	Note1
VDDB	CRUCQ12LHK6A125V	CONQUER ELECTRONICS Co.,Ltd.	6.0A 63V	18.0A, 3 seconds maximum	

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



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*1 In terms of voltage variation (voltage drop) while VDD rising edge is below 4.5 V, a protection circuit may work, and then this product may not work.

*2 These signals should be measured at the terminal of 100 Ω resistances.

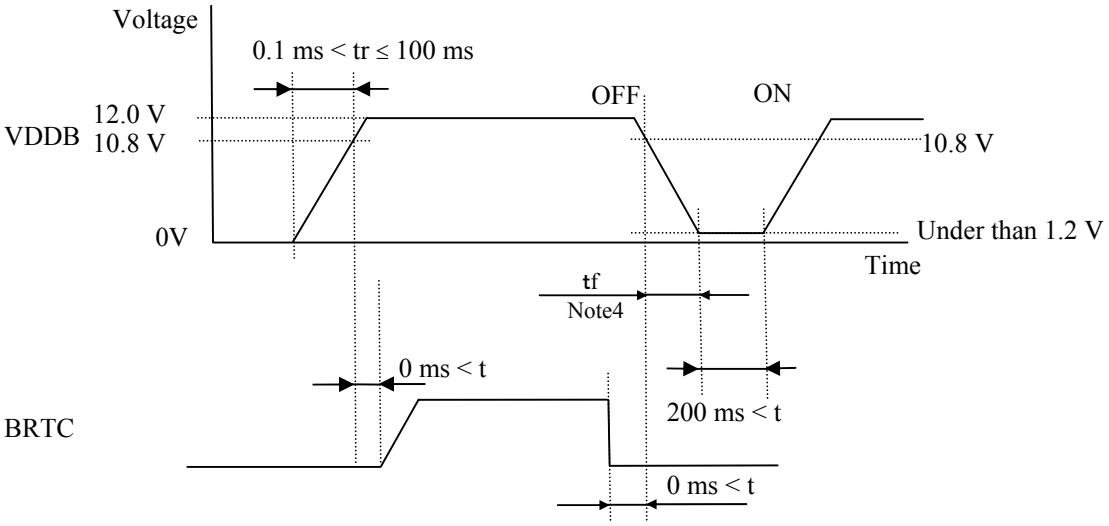
Note1: Display signals (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-) and TxSEL signal must be "0" voltage, exclude the VALID period (See above sequence diagram). If these signals are higher than 0.3V, the internal circuit is damaged.
If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note2: VDD should be 4.5 V or more while VDD ON period.

Note3: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.

Note4: Tf must be less than or equal to Tr in order to avoid any damage to the internal circuit. 5

4.4.2 LED driver board



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.
Note2: If tr is more than 100 ms, the backlight will be turned off by a protection circuit for LED driver board.
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open
Note4: tf must be less than or equal to tr in order to avoid any damage to the internal circuit.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-X30SSL-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-X30C series/ FI-X30H series/ FI-X30M series
(Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	DA0-	Odd pixel data 0	Note1
2	DA0+		
3	DA1-	Odd pixel data 1	Note1
4	DA1+		
5	DA2-	Odd pixel data 2	Note1
6	DA2+		
7	GND	Ground	Note2
8	CKA-	Odd pixel clock	Note1
9	CKA+		
10	DA3-	Odd pixel data 3	Note1
11	DA3+		
12	DB0-	Even pixel data 0	Note1
13	DB0+		
14	GND	Ground	Note2
15	DB1-	Even pixel data 1	Note1
16	DB1+		
17	GND	Ground	Note2
18	DB2-	Even pixel data 2	Note1
19	DB2+		
20	CKB-	Even pixel clock	Note1
21	CKB+		
22	DB3-	Even pixel data 3	Note1
23	DB3+		
24	GND	Ground	Note2
25	TxSEL	Selection of LVDS data input map	Open: Mode A Low: Mode B Note3, Note4
26	RSVD	-	Keep this pin Open.
27	N.C.	-	Keep this pin Open.
28	VDD	Power supply	Note2
29			
30			

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
Note2: All GND and VDD terminals should be used without any non-connected lines.
Note3: TxSEL is pulled-up in the product. (Pull-up resistance: 10kΩ)
Note4: See "**4.7 SELECTION OF LVDS DATA INPUT MAP**".

4.5.2 LED driver board

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co,.Ltd.)
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co,.Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

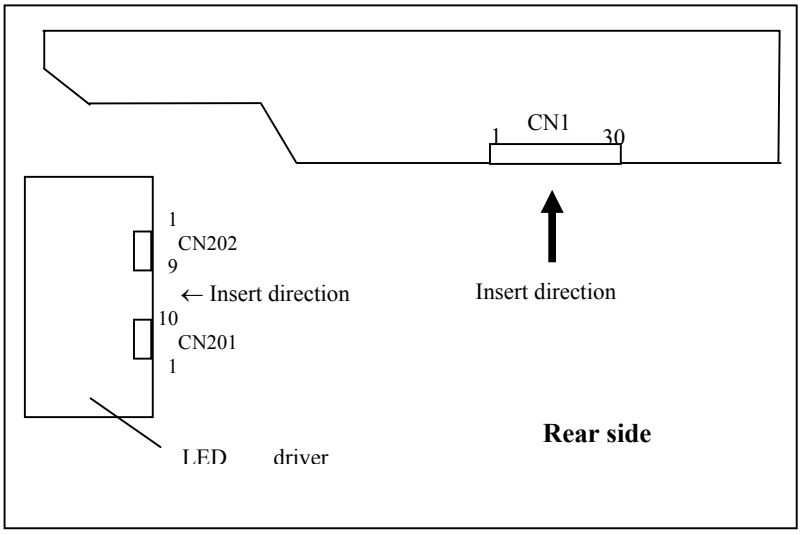
Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	LED driver board ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "**4.6 LUMINANCE CONTROL** ".
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

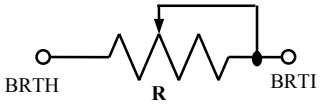
4.5.3 Positions of plug and socket



4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

(Ta=25°C) 5

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal
Variable resistor control Note1	• Adjustment The variable resistor (**R**) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance. The resistor (**R**) must be connected between BRTH-BRTI terminals.  • Luminance ratio Note3 Resistance / Luminance ratio 1 kΩ Note4 / 10% (typ.) 10 kΩ / 100% (Max. Luminance)	High or Open	Open
Voltage control Note1	• Adjustment Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open • Luminance ratio Note3 BRTI Voltage (VBI) / Luminance ratio 0.1 V Note4 / 10% (typ.) 1.0 V / 100% (Max. Luminance)		
Pulse width modulation Note1 Note2 Note5	• Adjustment Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal. • Luminance ratio Note3 Duty ratio / Luminance ratio 0.01 / 1% (typ.) (At frequency: 325 Hz) 1.0 / 100% (Max. Luminance)	Low	BRTP signal

5 5 5 5

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.
Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

Note3: These data are the target values.

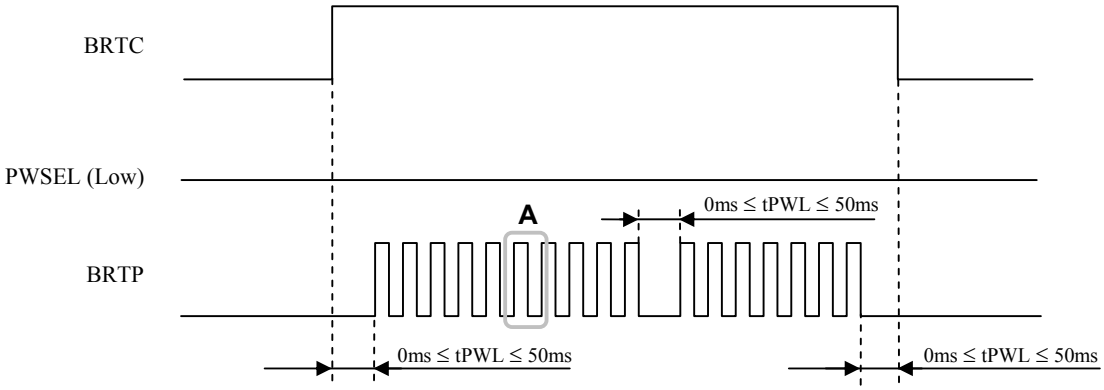
Note4: Do not set the variable resistor is less than 1kΩ or BRTI voltage is less than 0.1V.Otherwise flickers may cause or the LED may be turned off. 5

Note5: See "**4.6.2 Detail of BRTP timing**".

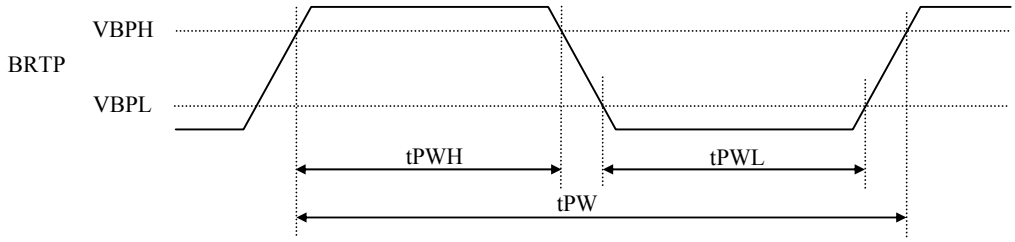
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Outline chart



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	f_{PWM}	185	-	1k	Hz	Note1,2,3
PWM duty ratio	DR_{PWM}	1	-	100	%	Note4,5
PWM pulse width	tPWH	30	-	-	μs	Note1,4,5

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW} \quad , DL = \frac{tPWH}{tPW}$$

Note2: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, a noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than 30μs. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

4.7 SELECTION OF LVDS DATA INPUT MAP

4.7.1 Mode A

	Input data	Note1		Transmitter Pin	THC63LVDM83D or equivalent		Transmitter Pin	THC63LVD823 or equivalent		Note2	CN1 Pin	CN1 Symbol
Odd pixel data and control signal		RA0	→	51	TA0		53	R12				
		RA1	→	52	TA1		54	R13	TA1-	→	1	DA0-
		RA2	→	54	TA2		57	R14	TA1+	→	2	DA0+
		RA3	→	55	TA3		58	R15				
		RA4	→	56	TA4		59	R16	TB1-	→	3	DA1-
		RA5	→	3	TA5		60	R17	TB1+	→	4	DA1+
		GA0	→	4	TA6		63	G12				
		GA1	→	6	TB0		64	G13	TC1-	→	5	DA2-
		GA2	→	7	TB1		65	G14	TC1+	→	6	DA2+
		GA3	→	11	TB2		66	G15			7	GND
		GA4	→	12	TB3		67	G16	TCLK1-	→	8	CKA-
		GA5	→	14	TB4		68	G17	TCLK1+	→	9	CKA+
		BA0	→	15	TB5		73	B12				
		BA1	→	19	TB6		74	B13	TD1-	→	10	DA3-
		BA2	→	20	TC0	1st	75	B14	TD1+	→	11	DA3+
		BA3	→	22	TC1		76	B15				
		BA4	→	23	TC2		77	B16				
		BA5	→	24	TC3		78	B17				
	Note3	RSVD	→	27	TC4		7	RSVD				
	Note3	RSVD	→	28	TC5		8	RSVD				
		DE	→	30	TC6		9	DE				
		RA6	→	50	TD0		51	R10				
		RA7	→	2	TD1		52	R11				
		GA6	→	8	TD2		61	G10				
		GA7	→	10	TD3		62	G11				
		BA6	→	16	TD4		69	B10				
		BA7	→	18	TD5		70	B11				
	Note3	RSVD	→	25	TD6		-					
		CLK	→	31	CLKIN		10	CLK				
Even pixel data		RB0	→	51	TA0		81	R22				
		RB1	→	52	TA1		82	R23	TA2-	→	12	DB0-
		RB2	→	54	TA2		83	R24	TA2+	→	13	DB0+
		RB3	→	55	TA3		84	R25			14	GND
		RB4	→	56	TA4		85	R26	TB2-	→	15	DB1-
		RB5	→	3	TA5		86	R27	TB2+	→	16	DB1+
		GB0	→	4	TA6		91	G22			17	GND
		GB1	→	6	TB0		92	G23	TC2-	→	18	DB2-
		GB2	→	7	TB1		93	G24	TC2+	→	19	DB2+
		GB3	→	11	TB2		94	G25				
		GB4	→	12	TB3		95	G26	TCLK2-	→	20	CKB-
		GB5	→	14	TB4		96	G27	TCLK2+	→	21	CKB+
		BB0	→	15	TB5		99	B22				
		BB1	→	19	TB6		100	B23	TD2-	→	22	DB3-
		BB2	→	20	TC0	2nd	1	B24	TD2+	→	23	DB3+
		BB3	→	22	TC1		2	B25			24	GND
		BB4	→	23	TC2		5	B26			25	TxSEL
		BB5	→	24	TC3		6	B27			26	RSVD
	Note3	RSVD	→	27	TC4		-				27	N.C.
	Note3	RSVD	→	28	TC5		-				28	VDD
	Note3	RSVD	→	30	TC6		-				29	VDD
		RB6	→	50	TD0		79	R20			30	VDD
		RB7	→	2	TD1		80	R21				
		GB6	→	8	TD2		89	G20				
		GB7	→	10	TD3		90	G21				
		BB6	→	16	TD4		97	B20				
		BB7	→	18	TD5		98	B21				
	Note3	RSVD	→	25	TD6		-					
		CLK	→	31	CLKIN		-					

4.7.2 Mode B

Input data			Transmitter Pin	THC63LVDM83D or equivalent		Transmitter Pin	THC63LVD823 or equivalent			CN1 Pin	CN1 Symbol
Odd pixel data and control signal		RA2 →	51	TA0		53	R12		Note2		
		RA3 →	52	TA1		54	R13	TA1- →		1	DA0-
		RA4 →	54	TA2		57	R14	TA1+ →		2	DA0+
		RA5 →	55	TA3		58	R15				
		RA6 →	56	TA4		59	R16	TB1- →		3	DA1-
		RA7 →	3	TA5		60	R17	TB1+ →		4	DA1+
		GA2 →	4	TA6		63	G12				
		GA3 →	6	TB0		64	G13	TC1- →		5	DA2-
		GA4 →	7	TB1		65	G14	TC1+ →		6	DA2+
		GA5 →	11	TB2		66	G15			7	GND
		GA6 →	12	TB3		67	G16	TCLK1- →		8	CKA-
		GA7 →	14	TB4		68	G17	TCLK1+ →		9	CKA+
		BA2 →	15	TB5		73	B12				
		BA3 →	19	TB6		74	B13	TD1- →		10	DA3-
		BA4 →	20	TC0	1st	75	B14	TD1+ →		11	DA3+
		BA5 →	22	TC1		76	B15				
		BA6 →	23	TC2		77	B16				
		BA7 →	24	TC3		78	B17				
	Note3	RSVD →	27	TC4		7	RSVD				
	Note3	RSVD →	28	TC5		8	RSVD				
		DE →	30	TC6		9	DE				
		RA0 →	50	TD0		51	R10				
		RA1 →	2	TD1		52	R11				
		GA0 →	8	TD2		61	G10				
		GA1 →	10	TD3		62	G11				
		BA0 →	16	TD4		69	B10				
		BA1 →	18	TD5		70	B11				
	Note3	RSVD →	25	TD6		-					
		CLK →	31	CLKIN		10	CLK				
Even pixel data		RB2 →	51	TA0		81	R22				
		RB3 →	52	TA1		82	R23	TA2- →		12	DB0-
		RB4 →	54	TA2		83	R24	TA2+ →		13	DB0+
		RB5 →	55	TA3		84	R25			14	GND
		RB6 →	56	TA4		85	R26	TB2- →		15	DB1-
		RB7 →	3	TA5		86	R27	TB2+ →		16	DB1+
		GB2 →	4	TA6		91	G22			17	GND
		GB3 →	6	TB0		92	G23	TC2- →		18	DB2-
		GB4 →	7	TB1		93	G24	TC2+ →		19	DB2+
		GB5 →	11	TB2		94	G25				
		GB6 →	12	TB3		95	G26	TCLK2- →		20	CKB-
		GB7 →	14	TB4		96	G27	TCLK2+ →		21	CKB+
		BB2 →	15	TB5		99	B22				
		BB3 →	19	TB6		100	B23	TD2- →		22	DB3-
		BB4 →	20	TC0	2nd	1	B24	TD2+ →		23	DB3+
		BB5 →	22	TC1		2	B25			24	GND
		BB6 →	23	TC2		5	B26			25	TxSEL
		BB7 →	24	TC3		6	B27			26	RSVD
	Note3	RSVD →	27	TC4		-				27	N.C.
	Note3	RSVD →	28	TC5		-				28	VDD
	Note3	RSVD →	30	TC6		-				29	VDD
		RB0 →	50	TD0		79	R20			30	VDD
		RB1 →	2	TD1		80	R21				
		GB0 →	8	TD2		89	G20				
		GB1 →	10	TD3		90	G21				
		BB0 →	16	TD4		97	B20				
		BB1 →	18	TD5		98	B21				
	Note3	RSVD →	25	TD6		-					
		CLK →	31	CLKIN		-					

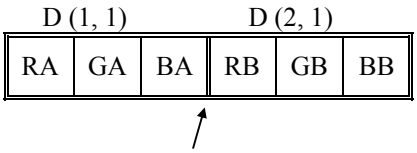
Note1: LSB (Least Significant Bit) – RA0, GA0, BA0, RB0, GB0, BB0
MSB (Most Significant Bit) – RA7, GA7, BA7, RB7, GB7, BB7
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																											
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.9 DISPLAY POSITION



D(1, 1)	D(2, 1)	•••	D(1280, 1)
D(1, 2)	D(2, 2)	•••	D(1280, 2)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(1,1024)	D(2, 1024)	•••	D(1280, 1024)

4.10 INPUT SIGNAL TIMINGS

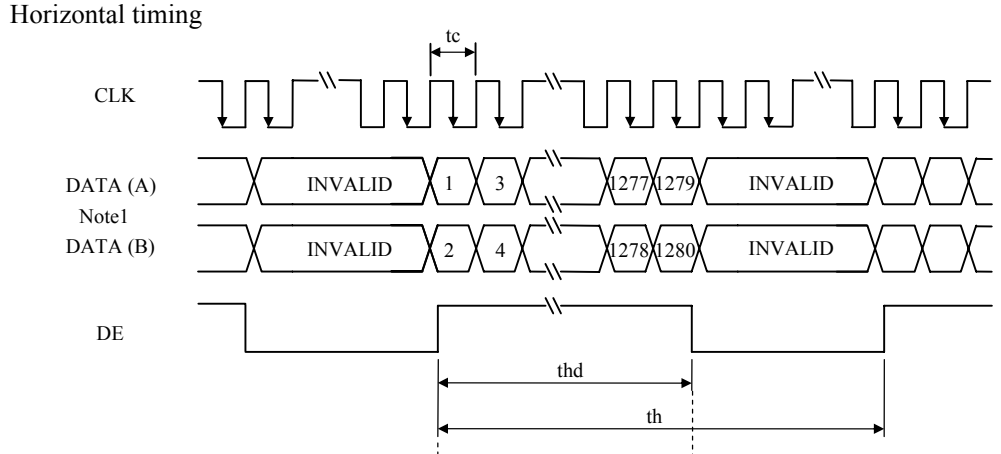
4.10.1 Timing characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	49	54	59	MHz	18.52 ns (typ.)
	Duty		-		-		-	Note2
	Rise time, Fall time		-				ns	
DATA	CLK-DATA	Setup time	-		-		ns	Note2
		Hold time	-				ns	
	Rise time, Fall time		-				ns	
DE	Horizontal	Cycl	th	12.3	15.63	20.59	µs	64.0 kHz (typ.) Note1, Note2
				660	844	1,024	CLK	
		Display period	thd	640			CLK	
	Vertical (One frame)	Cycle	tv	13.1	16.6	20.0	ms	60.0 Hz (typ.) Note1
				1,030	1,066	1,422	H	
		Display period	tvd	1,024			H	
	CLK-DE	Setup time	-		-		ns	Note2
		Hold time	-				ns	
	Rise time, Fall time		-				ns	

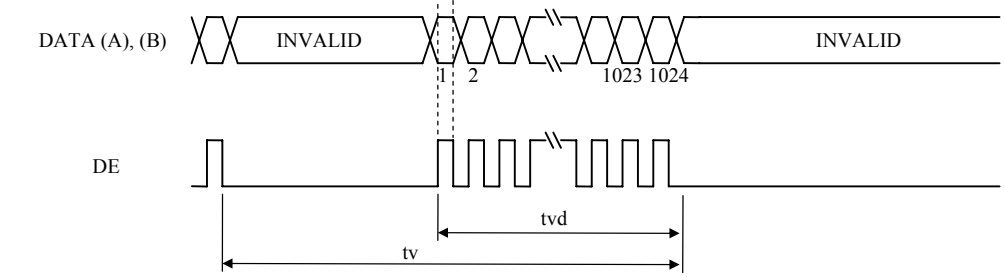
Note1: Definition of parameters is as follows.
tc = 1CLK, th = 1H
Note2: See the data sheet of LVDS transmitter.

4.10.2 Input signal timing chart

Horizontal timing



Vertical timing



Note1: DATA (A) = RA0-RA7, GA0-GA7, BA0-BA7
DATA (B) = RB0-RB7, GB0-GB7, BB0-BB7

4.11 OPTICS

4.11.1 Optical characteristics

(Note1, Note2)

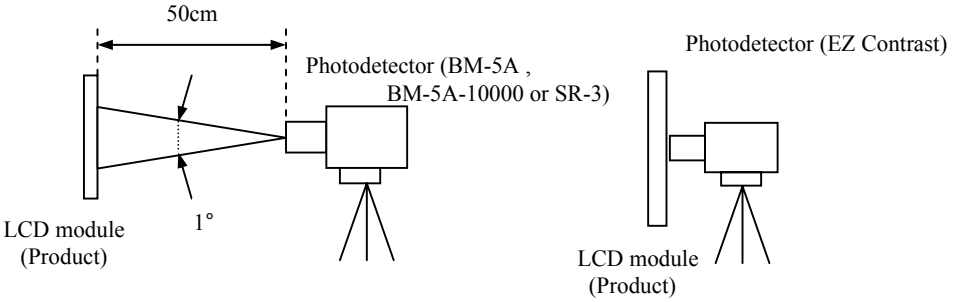
Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	600	800	-	cd/m^2	BM5A or SR-3	-
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	750	1000	-	-	BM5A or SR-3	Note3
Luminance uniformity		White θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU	-	1.1	1.25	-	BM-5A	Note4
Chromaticity	White	**x** coordinate	Wx	0.250	0.300	0.350	-	SR-3	Note5
		y coordinate	Wy	0.265	0.315	0.365	-		
	Red	**x** coordinate	Rx	0.590	0.640	0.690	-		
		y coordinate	Ry	0.280	0.330	0.380	-		
	Green	**x** coordinate	Gx	0.250	0.300	0.350	-		
		y coordinate	Gy	0.570	0.620	0.670	-		
	Blue	**x** coordinate	Bx	0.100	0.150	0.200	-		
		y coordinate	By	0.010	0.060	0.110	-		
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	65	72	-	%		
Response time		Black to white	Ton	-	14	25	ms	BM-5A -10000	Note6 Note7
		White to black	Toff	-	11	15	ms		
Viewing angle	Right	θU = 0°, θD = 0°, CR ≥ 10	θR	70	88	-	°	BM-5A, EZ Contrast	Note8
	Left	θU = 0°, θD = 0°, CR ≥ 10	θL	70	88	-	°		
	Up	θR = 0°, θL = 0°, CR ≥ 10	θU	70	88	-	°		
	Down	θR = 0°, θL = 0°, CR ≥ 10	θD	70	88	-	°		

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 5.0V, VDDB = 12.0V, At the maximum luminance control,
Display mode: SXGA, Horizontal cycle = 1/64.0kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "**4.11.2 Definition of contrast ratio**".

Note4: See "**4.11.3 Definition of luminance uniformity**".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = 35°C

Note7: See "**4.11.4 Definition of response times**".

Note8: See "**4.11.5 Definition of viewing angles**".

4.11.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

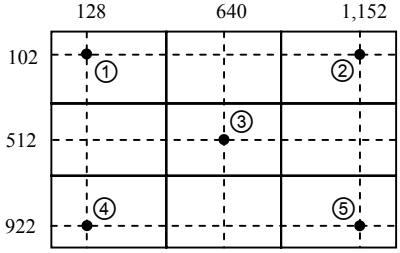
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.11.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

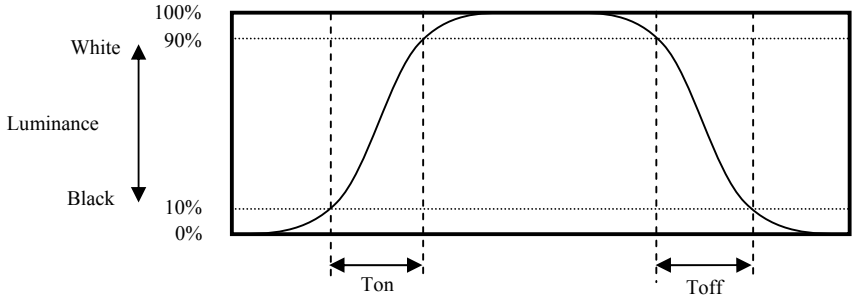
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

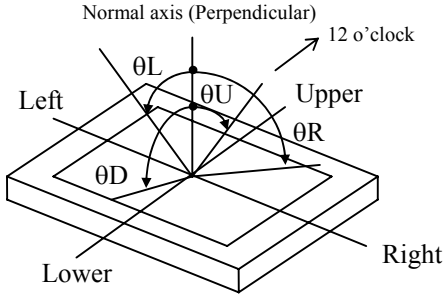


4.11.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.11.5 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

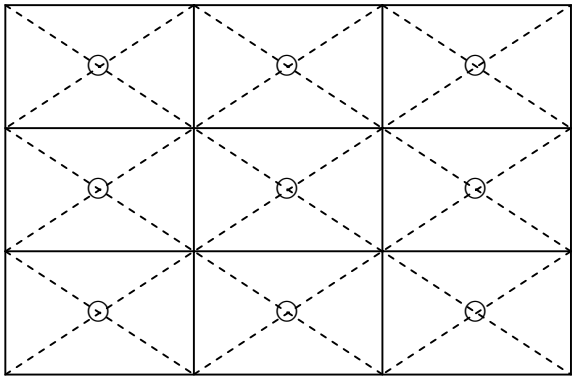
Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h

Note1: Life time expectancy is mean time to half-luminance.
Note2: Estimated luminance lifetime is not the value for LCD module but the value for LED elementary substance.
Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

6. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH = 90%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)		① -20 ± 3°C…1hour 70 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)		① -30 ± 3°C…30minutes 80 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/ s^2, 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±15kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Low pressure	Non-operation	① 15 kPa ② -30°C±3°C…24 hours ③ 80°C±3°C…24 hours	
	Operation	① 53.3 kPa ② -20°C±3°C…24 hours ③ 70°C±3°C…24 hours	

Note1: Display functions are checked under the same conditions as product inspection.
Note2: See the following figure for discharge points



7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**

⚠	This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.
☞	This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS

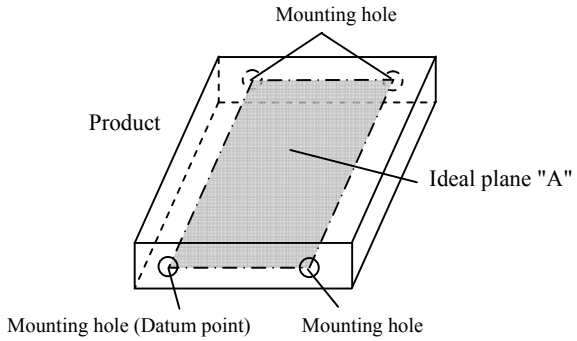
☞

- **Do not touch the working backlight. There is a danger of burn injury.**
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6 N (ϕ16mm jig))**

7.3 ATTENTIONS ⚠

7.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② When the product is put on the table temporarily, display surface must be placed downward.
③ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
④ The torque for product mounting screws must never exceed 0.67N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws from surface of plate (product side) must be ≤ 3.0 mm
⑤ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



⑥ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
⑦ Do not push or pull the interface connectors while the product is working.
⑧ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑨ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
③ Do not operate in high magnetic field. If not, circuit boards may be broken.
④ This product is not designed as radiation hardened.

7.3.3 Characteristics

The following items are neither defects nor failures.

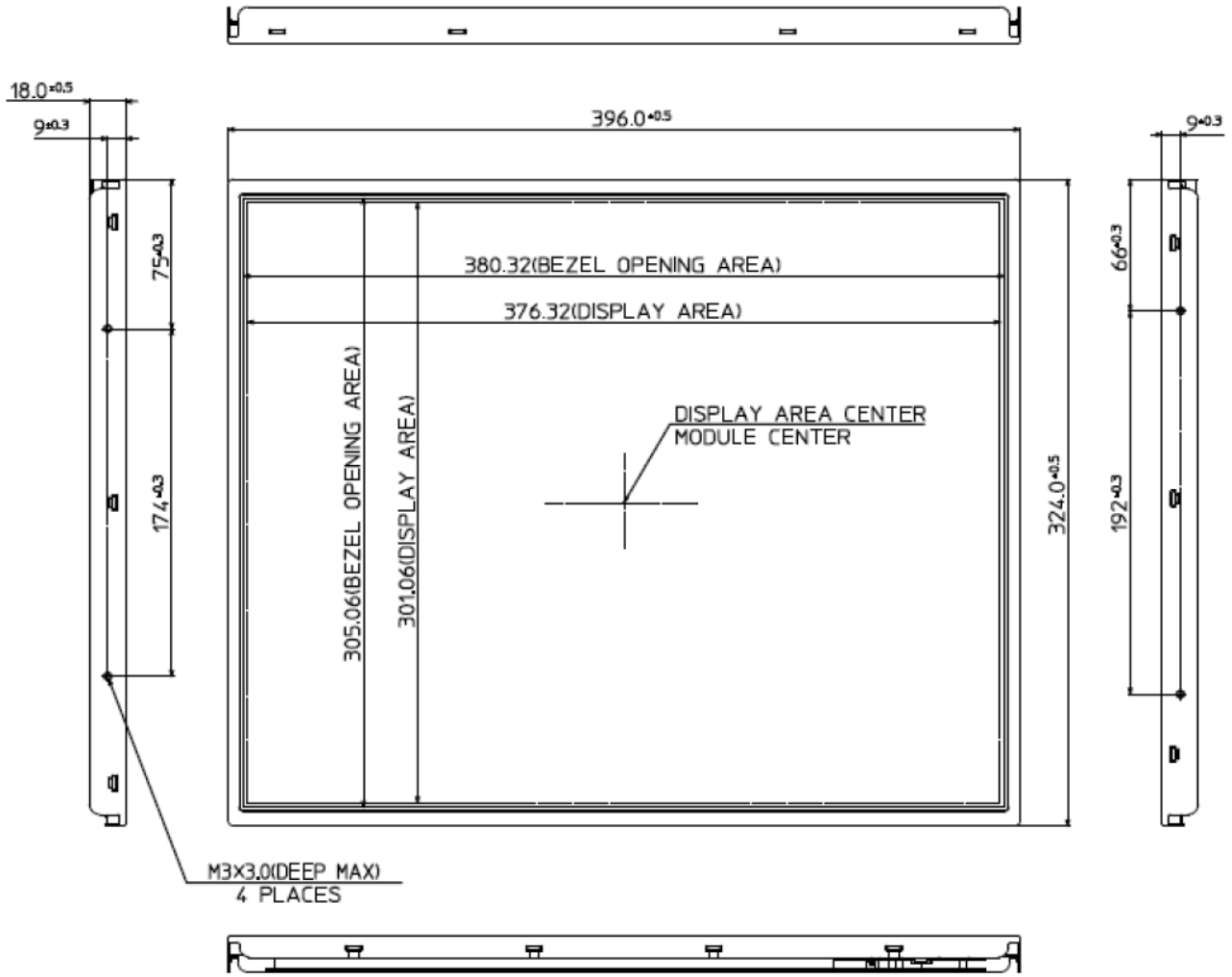
① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑥ Optical characteristics may be changed depending on input signal timings.
⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the LED driver board may appear on a display. Set up luminance control frequency of the LED driver board so that the interference noise does not appear.

7.3.4 Others

① All GND, VDD, GNDB and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.
④ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.

8. OUTLINE DRAWINGS

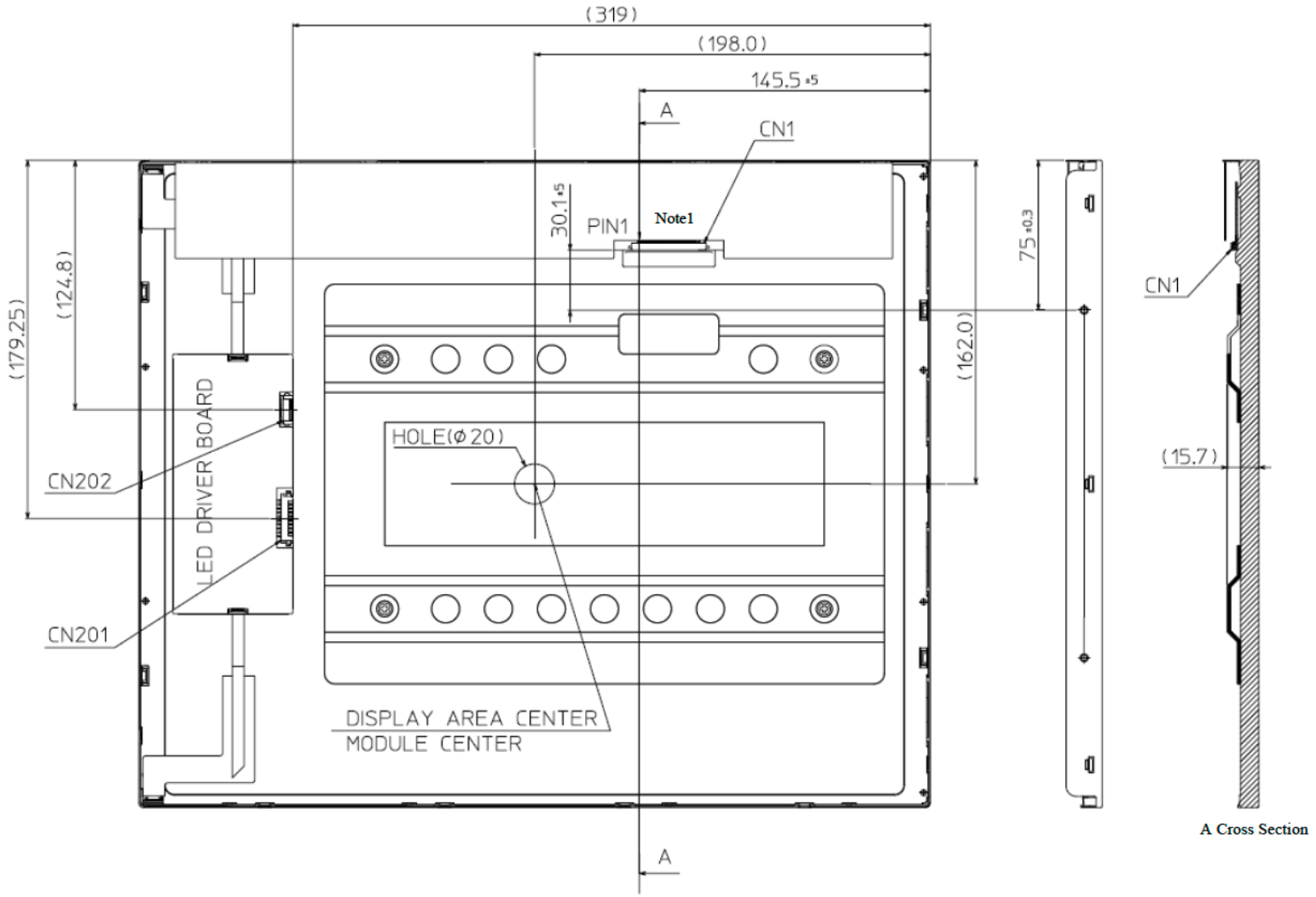
8.1 FRONT VIEW



Note1: The values in parentheses are for reference.
Note2: The torque for product mounting screws must never exceed 0.67N·m.

Unit: mm

8.2 REAR VIEW



Note1: Connector keep-out area 55×44mm edge is located 4mm from Pin1 keep out area is shown in cross-hatch.
Note2: The torque for product mounting screws must never exceed 0.67N·m.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-1453	July 9, 2012	**Revision contents** New issue **Writer** *Approved by* T. OGAWA *Checked by* *Prepared by* E. YOSHIMURA
2nd edition	DOD-PP-1517	Nov. 16, 2012	**Revision contents** P5 GENERAL SPECIFICATIONS • Module size: TBD (D) (typ.) mm → 22.0 (D) (max.) mm • Polarizer pencil-hardness: (2H) (min.) → 2H (min.) • Luminance: 600 cd/m^2 (min.) → (800) cd/m^2 (typ.) • < (30.0) W (typ.) → (45.0) W (typ.) P6 BLOCK DIAGRAM • TxSEL - VDD: TBD Ω → TxSEL - VDD: (10k)Ω P7 ABSOLUTE MAXIMUM RATINGS • Power supply voltage - LCD panel signal processing board: TBD V → -0.3 to +6.5 V - LED driver: TBD V → -0.3 to +25.0 V • Input voltage for signals - Display signals: TBD V → -0.3 to +2.4 V - Function signals: TBD V → -0.3 to +3.3 V - Function signal for LED driver - BRTC: TBD V → -0.3 to +6.3 V - BRTI: TBD V → -0.3 to +6.0 V - BRTP: TBD V → -0.3 to +5.5 V - PWSEL: TBD V → -0.3 to +6.5 V • Note3,4: center of (elimination) P8 LCD panel signal processing board • Power supply voltage: TBD (min., max.) V → 4.5 (min.), 5.5 (max.) V • Power supply current: TBD (typ., max.) mA → (700) (typ.), (900) (max.) mA • Input voltage for TxSEL signal - Low: TBD (max.) V → (0.3) (max.) V • Note4:: TBDΩ → (10k)Ω P9 LED driver board • Power supply voltage: TBD (min., max.) V → 10.8 (min.), 13.2 (min.) V • Power supply current: TBD (typ., max.) mA → (3,300) (typ.), (3,700) (max.) mA • Input voltage for signals - BRTI signal: TBD (min., max.) V→ 0 (min.), 1.0 (max.) V - BRTP signal - High: TBD (min., max.) V → (2.0) (min.), (5.0) (max.) V - Low: TBD (min., max.) V → 0 (min.), (0.8) (max.) V - BRTC signal - High: TBD (min., max.) V → (1.8) (min.), (5.0) (max.) V - Low: TBD (min., max.) V → 0 (min.), (0.6) (max.) V - PWSEL signal - High: TBD (min., max.) V → (2.1) (min.), (3.3) (max.) V - Low: TBD (min., max.) V → 0 (min.), (0.9) (max.) V P9 LED driver board current wave • Push peak current: TBD mA → (4,000) mA P10 Fuse • VDD, VDDB: TBD → specified

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
2nd edition	DOD-PP-1517	Nov. 16, 2012	**Revision contents** P11 LCD panel signal processing board (Revised) • TBD V → 4.0 V (2points) • TBD V → 4.5 V (2points) • TBD ms < Tr < TBD ms → 0.1 ms < Tr < 80 ms • Toff > TBD ms → Toff > 200 ms • TBD ms < t < TBD ms → 10 ms < t < 35 ms (2points) • *1: TBD V → 4.5V • Note2: TBD V → 4.5V P12 LED driver board (Revised) • TBD ms < tr ≤ TBD ms → 0.1 ms < tr ≤ 100 ms • TBD V → 12.0 V • TBD V → 11.4 V (2points) • TBD V → 1.2 V • TBD ms < 1 → 0 ms < 1 (2points) • TBD ms < 1 → 200 ms < 1 • Note2: TBD ms → 100 ms P13 LCD panel signal processing board • Note3: TBDΩ → (10k)Ω P15 Luminance control methods • Variable resistor control (addition) • Voltage control (addition) • Pulse width modulation: Luminance ratio - TBD Hz → 325 Hz P16 Detail of BRTP timing - Each parameter • Luminance control frequency (FL) → PWM frequency (f_{PWM}) (change of expression) • External PWM pulse width (tPWH) → PWM pulse width (tPWH) (change of expression) • PWM frequency: TBD (min., max.) Hz → (185) (min.), (1000) (max.) Hz • PWM duty ratio (addition) • PWM pulse width: TBD (min.) μs → (30) (min.) μs • Note2 See the following…. (elimination) • Note3 See "4.6.1…(elimination) • Note2-5 (addition) P22 Optical characteristics • Luminance: TBD (typ.) cd/m^2 → (800) (typ.) cd/m^2 • Chromaticity - (Rx, Ry): TBD (typ.) → ((0.640), (0.330)) (typ.) - (Gx, Gy): TBD (typ.) → ((0.300), (0.620)) (typ.) - (Bx, By): TBD (typ.) → ((0.150), (0.060)) (typ.) • Response time - Ton: TBD (typ.) ms → (14) (typ.) ms - Toff: TBD (typ.) ms → (11) (typ.) ms P26 CAUTIONS • 539 m/s^2 → 294 m/s^2 (correction) P28 OUTLINE DRAWINGS - FRONT VIEW • TBD → 22.0 (max.) P29 OUTLINE DRAWINGS - REAR VIEW • .(319.0) , (124.8) ,(179.25) (addition) • 198.0 , 162.0 (addition) **Writer** *Approved by* K. FUJIMOTO *Checked by* *Prepared by* E. YOSHIMURA

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
3rd edition	DOD-PP-1554	Jan. 25, 2013	**Revision contents** P6 BLOCK DIAGRAM • LED driver board: DC/DC Converter, VDDB-PWSEL, VDDB-BRTC (addition) P10 Fuse • VDDB: CRUCQ12LVK4.0A125V, CRUCQ12LVK2.5A125V (elimination) P11 LCD panel signal processing board • VDD: 4.0V → 0 V P28 OUTLINE DRAWINGS - FRONT VIEW • 380.32(BEZEL OPENING AREA) (addition) • 305.06(BEZEL OPENING AREA) (addition) P29 REAR VIEW (Revised) • A Cross Section (addition) • 198.0 → (198.0) • 162.0 → (162.0) • 30.1+5 → 30.1±5 **Writer** *Approved by* K. FUJIMOTO *Checked by* ——— *Prepared by* E. YOSHIMURA
4th edition	DOD-PP-1694	June 21, 2013	**Revision contents** CORRECTION OF DESCRIPTIVE CONTENTS P5 General Specifications • Module size: 22.0 (D) (max.) mm → 18.0 (D) (typ.) mm • Weight: TBD g (typ.) → (2,100) (typ.), (2,310) (max.) g • Contrast ratio: (1000):1(typ.) → 1000:1(typ.) • Luminance: (800) cd/m^2 (typ.) → 800 cd/m^2 (typ.) P6 Block Diagram • TxSEL - VDD: (10kΩ) → 10 kΩ • PESEL, BRTC - DC/DC Converter: (1k) Ω → 1 kΩ P7 Detailed specifications - Mechanical specifications • Module size: TBD (D) (typ.) mm → 18.0 ± 0.5 (D) (typ.) mm • Weight: TBD (typ.) → (2,100) (typ.) , (2,310) (max.) g P8 LCD panel signal processing board • Power supply current: (700), (900) (typ., max.) mA → 700(typ.), 900 (max.) mA • Input voltage for TxSEL signal - Low: (0.3) (max.) V → 0.9 (max.) V • Input current for TxSEL signal: TBD (typ., max.) μA→ -10 (typ.), 10 (max.) μA • Note4: (10kΩ) → 10 kΩ P9 LED driver board • Power supply current: (3,300), (3,700) (typ., max.) →(3,460), (4,020) • Input voltage for signals - VBPH: (2.0) (typ.), (5.0) (max.) V → 2.0 (typ.), 5.0 (max.) V - VBPL: (0.8) (max.) V → 0.8 (max.) V - VBCH: (1.8) (typ.), (5.0) (max.) V → 2.0 (typ.), 5.0 (max.) V - VBCL: (0.6) (max.) V → 0.8 (max.) V - VBSH: (2.1) (typ.), (3.3) (max.) V → 2.5 (typ.), 3.3 (max.) V - VBSL: (0.9) (max.) V → 0.9 (max.) V • Input current for signals: Specified P9 LED driver board current wave • Push peak current: (4,000) mA → 4,000 mA P13 LCD panel signal processing board • Note3: (10kΩ) → 10 kΩ P16 Detail of BRTP timing - Each parameter • PWM frequency: (185) (min.), (1,000) (max.) Hz → 185 (min.), 1k (max.) Hz • PWM pulse width: (30) (min.) μs →30 (min.) μs P20 Timing characteristics • DE - Vertical - Cycle: 17.5 (max.) ms → 20.0 (max.) ms

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
4th edition	DOD-PP-1694	June 21, 2013	**Revision contents** P22 Optical characteristics • Luminance: (800) (typ.) → 800 (typ.) • Contrast ratio: TBD, (1000) (min., typ.) → (750), 1000 (min., typ.) • Chromaticity: Specified • Response time: Specified • Note6: TopF = (35)°C → TopF = 35°C P25 Reliability tests • Dust (elimination) P26 Handling of the product • ④ ≤ TBD mm → 3.0 mm P28 Outline Drawings • 22(MAX) mm → 18.0±0.5 mm **Writer** *Approved by* R. KAWASHIMA *Checked by* ——— *Prepared by* E. YOSHIMURA
5th edition	DOD-PP-1707	July 16, 2013	**Revision contents** P5 General Specifications • Weight: (2,100), (2,310) (typ., max.) g → 2,100, 2,310 (typ., max.) g • Power consumption (45.0)W (typ.) → 45.0W (typ.) P6 Block Diagram • TxSEL - VDD → TxSEL – DC/DC Converter P7 Mechanical Specifications • Weight: (2,100), (2,310) (typ., max.) g → 2,100, 2,310(typ., max.) g P8 LCD panel signal processing board • Input current for TxSEL signal: -10, 10 (min., max.) μA →-400, 400 (min., max.) μA P9 LED driver board • Power supply current: (3,460), (4,020) (typ., max.) mA → 3,460, 4,020 (typ., max.) mA • Input voltage for signals - VBI: 0 (min.) V → 0.1 (min.) V - VBPH: 2.0, 5.0 (min., max.) V → 2.3, 3.3 (min., max.) V - VBPL: 0.8 (max.) V → 0.6 (max.) V - VBCH: 2.0, 5.0 (min., max.) V → 2.3, 3.3 (min., max.) V - VBCL: 0.8 (max.) V → 0.6 (max.) V - VBSH: 2.5 (min.) V → 2.3 (min.) V P11 LCD panel signal processing board • Note4 (addition) P12 LED driver board • 11.4 V → 10.8 V (2points) • Note4 (addition) P15 Luminance control methods • Ta=25°C (addition) • Variable resistor control - Resistance: 0kΩ → 1kΩ - Luminance ratio: 0%(Min. Luminance) → 10% (typ.) • Voltage control - BRTI Voltage: 0V → 0.1V - Luminance ratio: 0%(Min. Luminance) → 10% (typ.) • Polse width modulation - Luminance ratio: 1%(Min. Luminance) → 1% (typ.) • Note4 (addition) P22 Optical characteristics • Contrast ratio: (750) (min.) → 750 (min.)

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
5th edition	DOD-PP-1707	July 16, 2013	**Revision contents** **Signature of writer** *Approved by* R. KAWASHIMA *Checked by* *Prepared by* E. YOSHIMURA