

**TENTATIVE**

All information in this technical data sheet is tentative  
and subject to change without notice.

**Preliminary**

**8.4" VGA**

**TECHNICAL SPECIFICATION**

**T-55467D084J-LW-A-AAN**

**OPTREX CORPORATION.**

Date: Nov.28,'08

# CONTENTS

| No. | Item                                    | Page          |
|-----|---|---------------|
| --  | COVER                                   | 1             |
| --  | CONTENTS                                | 2             |
| 1   | APPLICATION                             | 3             |
| 2   | OVERVIEW                                | 4             |
| 3   | ABSOLUTE MAXIMUM RATINGS                | 5             |
| 4   | ELECTRICAL CHARACTERISTICS              | 5, 6          |
| 5   | INTERFACE PIN CONNECTION                | 7, 8          |
| 6   | INTERFACE TIMING                        | 9, 10, 11, 12 |
| 7   | BLOCK DIAGRAM                           | 13            |
| 8   | MECHANICAL SPECIFICATION                | 14, 15        |
| 9   | OPTICAL CHARACTERISTICS                 | 16, 17, 18    |
| 10  | RELIABILITY TEST CONDITION              | 19            |
| 11  | OTHER FEATURE                           | 20            |
| 12  | HANDLING PRECAUTIONS FOR TFT-LCD MODULE | 21, 22, 23    |



## 2. OVERVIEW

T-55467D084J-LW-A-AAN is 8.4" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit, and backlight unit.

### 3. ABSOLUTE MAXIMUM RATINGS

| ITEM   | SYMBOL                    | MIN. | MAX. | UNIT |
|--|---------------------------|------|------|------|
| Power Supply Voltage for LCD                           | VCC                       | 0.3  | 4.0  | V    |
| Logic Input Voltage                                    | VI                        | 0.3  | 6.0  | V    |
| Backlight (LED) Current                                | IF                        | 0    | 180  | mA   |
| Operation Temperature (Panel) <small>Note 1,2)</small> | T <sub>op</sub> (Panel)   | 30   | 80   | °C   |
| Operation Temperature (Ambient) <small>Note 2)</small> | T <sub>op</sub> (Ambient) | 30   | 80   | °C   |
| Storage Temperature <small>Note 2)</small>             | T <sub>stg</sub>          | 30   | 80   | °C   |

[Note]

- 1) Measured at the center of active area and at the center of panel back surface
- 2) Top, Tstg > 40 C : 90%RH max. without condensation  
 Top, Tstg > 40 C : Absolute humidity shall be less than the value of 90%RH at 40 C without condensation.

### 4. ELECTRICAL CHARACTERISTICS

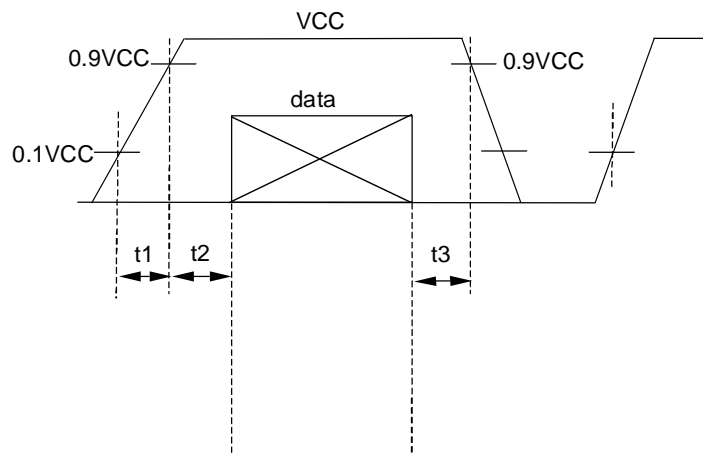
(1) TFT- LCD

Ambient Temperature: Ta = 25°C

| ITEM                             | SYMBOL | MIN. | TYP. | MAX. | UNIT  | Remarks     |
|----------------------------------|--------|------|------|------|-------|-------------|
| Power Supply Voltage for LCD     | VCC    | 3.0  | 3.3  | 3.6  | V     | *1)         |
| Power Supply Current for LCD     | ICC    | -    | 320  | 500  | mA    | *2)         |
| Permissible Input Ripple Voltage | VRP    | -    | -    | 100  | mVp-p | VCC = +3.3V |
| Logic Input Voltage              | High   | VIH  | 2.0  | -    | 5.5   | V           |
|                                  | Low    | VIL  | 0    | -    | 0.8   | V           |

\*1) Power and signals sequence:

|        |       |        |    |
|--------|-------|--------|----|
| t1     | 10 ms | 200 ms | t4 |
| 0 < t2 | 50 ms | 200 ms | t5 |
| 0 < t3 | 50 ms | 0      | t6 |

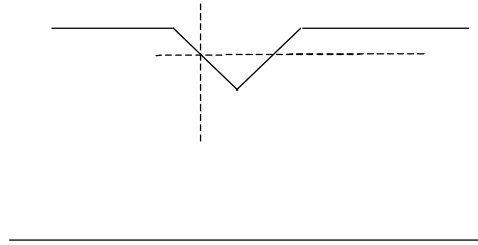


VCC-dip conditions:

1) When  $2.4\text{ V} < VCC < 3.0\text{ V}$ ,  $t_d = 10\text{ ms}$

2) When  $VCC < 2.4\text{ V}$

VCC-dip conditions should also follow the power and signals sequence.



under high temperature.

## 5. INTERFACE PIN CONNECTION

### (1) CN 1(Interface Signal)

Used connector: DF9BA-31P-1V(32) (HIROSE)

Corresponding connector: DF9B-31S-1V (HIROSE)

| Pin No. | Symbol | Function                                    |
|---------|--------|---|
| 1       | GND    |   |
| 2       | DCLK   | Clock signal for sampling catch data signal |
| 3       | HD     | Horizontal sync signal *1)                  |
| 4       | VD     | Vertical sync signal *1)                    |
| 5       | GND    |   |
| 6       | R0     | Red data signal(LSB)                        |



(2) CN 2(Backlight)

## 6. INTERFACE TIMING

### (1) Timing Specifications

| ITEM                |             | SYMBOL           | MIN.            | TYP. | MAX. | UNIT |                  |
|---------------------|-------------|------------------|-----------------|------|------|------|------------------|
| DCLK                | Frequency   | f <sub>CLK</sub> | 20              | 25   | 30   | MHz  |                  |
|                     | Period      | t <sub>CLK</sub> | 33.3            | 40   | 50   | ns   |                  |
|                     | Low Width   | t <sub>wCL</sub> | 10              | --   | --   | ns   |                  |
|                     | High Width  | t <sub>wCH</sub> | 10              | --   | --   | ns   |                  |
| DATA(R,G,B)<br>DENA | Set up time | t <sub>DS</sub>  | 4               | --   | --   | ns   |                  |
|                     | Hold time   | t <sub>DH</sub>  | 4               | --   | --   | ns   |                  |
| DENA                | Horizontal  | Active Time      | t <sub>HA</sub> | 640  | 640  | 640  | t <sub>CLK</sub> |
|                     |             | Blanking Time    | t <sub>HB</sub> | 20   | 160  | --   | t <sub>CLK</sub> |
|                     |             | Frequency        | f <sub>H</sub>  | 27   | 31.5 | 38   | kHz              |
|                     |             | Period           | t <sub>H</sub>  | 26.3 | 31.7 | 37.0 | s                |
|                     | Vertical    | Active Time      | t <sub>VA</sub> | 480  | 480  | 480  | t <sub>H</sub>   |
|                     |             | Blanking Time    | t <sub>VB</sub> | 4    | 45   | --   | t <sub>H</sub>   |
|                     |             | Frequency        | f <sub>V</sub>  | 55   | 60   | 70   | Hz               |
|                     |             | Period           | t <sub>V</sub>  | 14.3 | 16.7 | 18.2 | ms               |

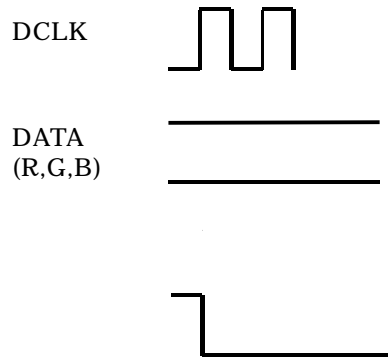
[Note]

- 1) DATA is latched at fall edge of DCLK in this specification.
- 2) DENA (Data Enable) should always be positive polarity as shown in the timing specification.
- 3) DCLK should appear during all invalid period.
- 4) In case of blanking time fluctuation, please satisfy following condition.

$$t_{VBn} > t_{VBn-1} - 3(t_H)$$

(2) Timing Chart

b. Horizontal Timing Chart



(3) Color Data Assignment

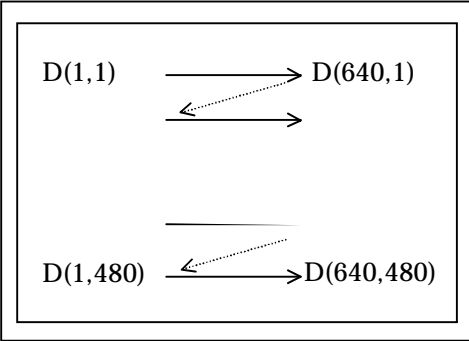
|       |            |    |    |    |    |     |        |    |    |    |    |     |        |    |    |     |    |    |
|-------|------------|----|----|----|----|-----|--------|----|----|----|----|-----|--------|----|----|-----|----|----|
| COLOR | INPUT DATA |    |    |    |    |     |        |    |    |    |    |     |        |    |    |     |    |    |
|       | R DATA     |    |    |    |    |     | G DATA |    |    |    |    |     | B DATA |    |    |     |    |    |
|       | R5         | R4 | R3 | R2 | R1 | R0  | G5     | G4 | G3 | G2 | G1 | G0  | B5     | B4 | B3 | B2  | B1 | B0 |
|       | MSB        |    |    |    |    | LSB | MSB    |    |    |    |    | LSB | MSB    |    |    | LSB |    |    |

(4) Display Position and Scan Direction

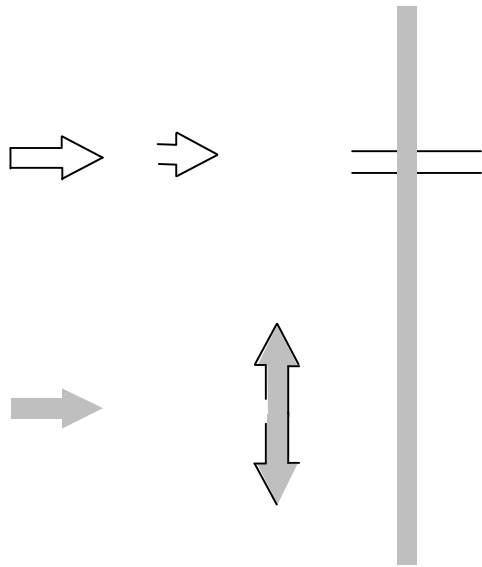
D(X,Y) shows the data number of input signal for LCD panel signal processing PCB.

SC: Low

SC: High



## 7. BLOCK DIAGRAM



# 8. MECHANICAL SPECIFICATIONS

## (1) Front Side







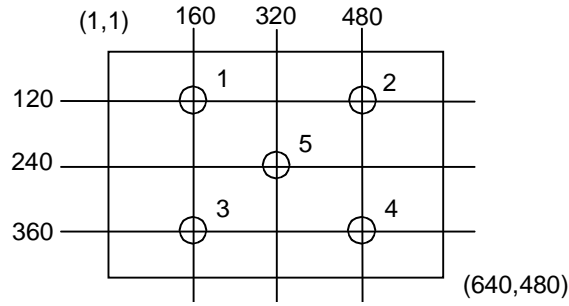
## 9. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, Input Signals: Typ. Values shown in Section 6

| ITEM           | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT | Remarks |
|----------------|--------|-----------|------|------|------|------|---------|
| Contrast Ratio | CR     | v         |      |      |      |      |         |

\*1) Measurement Point

Contrast Ratio, Luminance, Response Time, Viewing Angle, Color Coordinates: Display Center  
 Luminance Uniformity: point 1-5 shown in a figure below



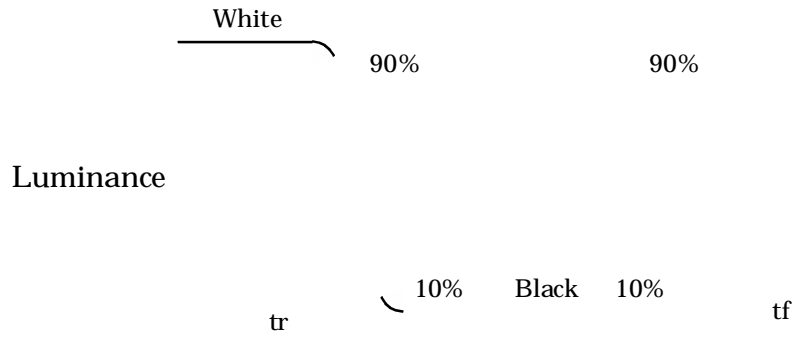
\*2) Definition of Contrast Ratio

$CR = \text{Luminance with all white pixels} / \text{Luminance with all black pixels}$

\*3) Definition of Luminance Uniformity

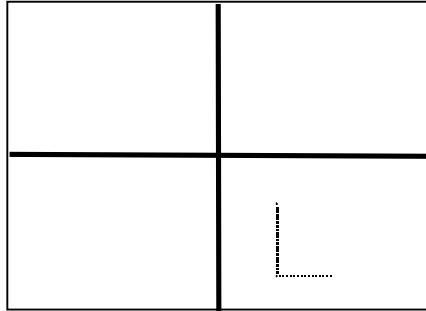
$$Lw = [Lw(\text{MAX}) / Lw(\text{MIN}) - 1] \cdot 100$$

\*4) Definition of Response Time



\*6) Image Sticking

Continuously display the test pattern shown in the figure below for two-hours. Then display a completely white screen. The previous image shall not persist more than two seconds at 25°C.



## 10. RELIABILITY TEST CONDITION

### (1) Temperature and Humidity

| TEST ITEM                                   | CONDITIONS                              |
|---|---|
| HIGH TEMPERATURE<br>HIGH HUMIDITY OPERATION | 40°C, 90%RH, 240 h<br>(No condensation) |
| HIGH TEMPERATURE OPERATION                  | 80°C, 240 h                             |

LOW TEM

## 11. OTHER FEATURE

This LCD module complies with RoHS<sup>\*)</sup> directive.

<sup>\*)</sup> RoHS: Restriction of the use of certain hazardous substances in electrical and electronic equipment

## 12. HANDLING PRECAUTIONS FOR TFT-LCD MODULE

Please pay attention to the followings in handling TFT-LCD products;

### (1) ASSEMBLY PRECAUTION

- a. Please mount the LCD module by using mounting hole with a screw clamping torque (recommended value: 0.3 Nm). Please do not bend or wrench the LCD module in assembling. Please do not drop, bend or twist the LCD module in handling.
- b. Please design display housing in accordance with the following guide lines.
  - (a) Housing case must be designed carefully so as not to put stresses on LCD and not to wrench module.



- d. LED driver should be designed carefully to limit or stop its function when over current is detected on the LED.

(6) OTHERS

- a. A strong incident light into LCD panel may cause deterioration to polarizer film, color filter, and other materials, which will degrade the quality of display characteristics. Please do not expose LCD module under strong Ultraviolet rays for a long time.
- b. Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
- c. For the packaging box handling, please see and obey with the packaging specification datasheet.