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Specification
ECX109AKN-6

Version: September 2014

SONY

19.80 cm Color OLED Panel Module

ECX109AKN-6

Description

The ECX109AKN-6 is a 19.80 cm (type 7.4) diagonal, 960 (H) × 540 (V) dots (518400 effective pixels) active matrix color OLED panel module using low temperature polycrystalline silicon transistors. This panel features high contrast ratio and high luminance. These features are achieved by adopting the microcavity structure and the top emission structure combined with color filters. In addition, an all solid-state structure enables high reliability. This module can realize high luminance, high contrast ratio and wide color range and various adjusted optical characteristics and function by controlling timing controller (Tcon) using I2C.

Features

◆ Number of effective pixels 960 (H) × 540 (V)

◆ Pixel pitch 171 μm (H) × 171 μm (V)

◆ Surface treatment AR (anti-reflection) coating film

◆ Thin and lightweight

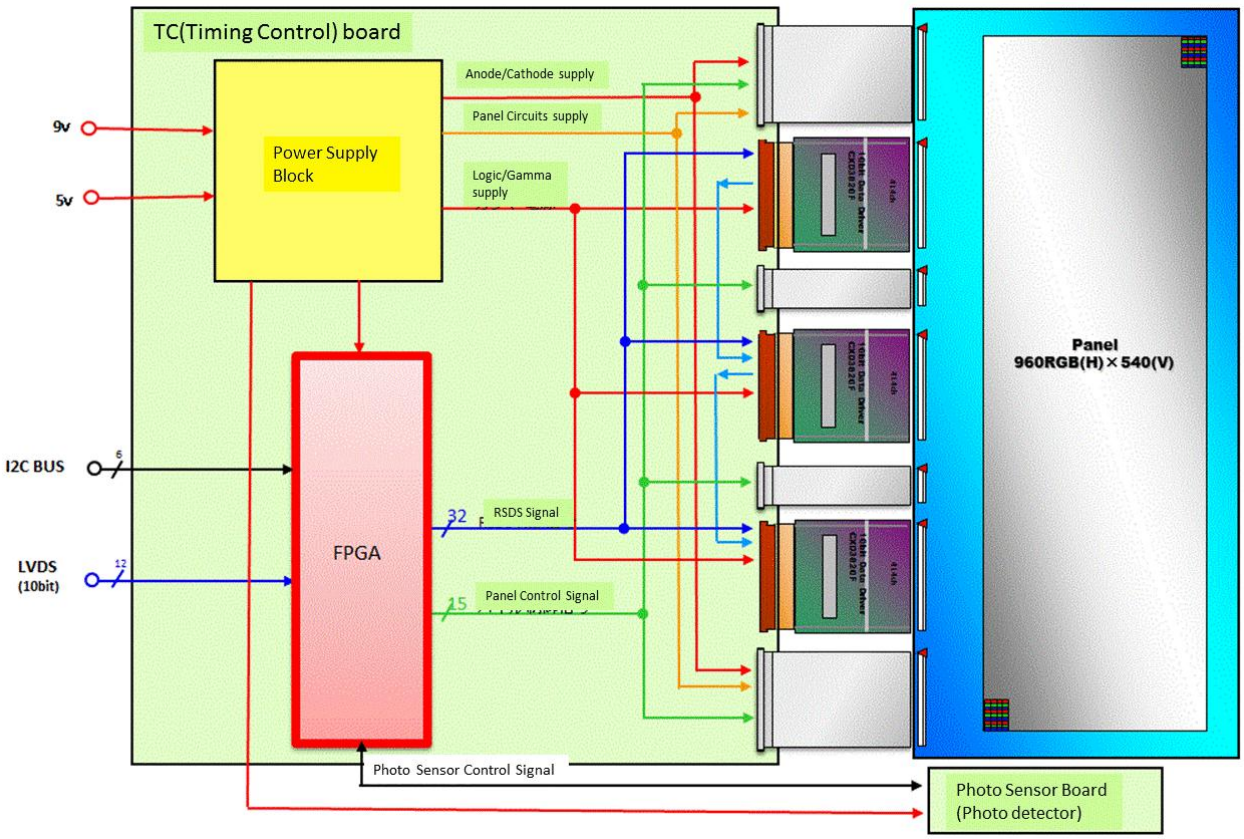
Element Structure

◆ Number of pixels

- ◆ Total number of pixels : 960 (H) × 540 (V) = 518400

◆ Module dimensions : 207.4 mm (H) × 121.0 mm (V) x 12.0 mm (H) (Typ.) , maximum thickness position 14.6 mm

Module Block Diagram



Module specifications

Item	Specification
Display area	7.4 inch (diagonal 19.80 cm) 164.160ｍｍ(H) × 92.340mm (V)
Package dimensions	207.4 mm (H) × 121.0 mm (V) × 12 mm (14.6 mm maximum thickness)
Pixel pitch	0.171 mm × 0.171 mm
Number of pixels	960 (H) × 540 (V) Quarter Full-HD
Number of gray scales	10 bit, 1,073741,824 colors
Luminance	350 cd/m^2or more (when inputting maximum gray scale)
Power consumption	9.3 W (typ. when displaying all white)
Weight	310 g (typ.)

Display structure	AMOLED top emission
Surface treatment	ARfilm Haze; 2 % Hardness; 2H

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Supply voltage	+9 V	14	V	CN101 *1
	+5V	6	V	CN101 *1
I2C control voltage	I2C_SDA, SCL・・・	3.6	V	All control pins in CN105
Operating temperature	Top	−10 to 55	℃	Panel surface temperature *2
Storage temperature	Tst	−30 to 60	℃	Ambient temperature
Operating humidity	Hop	10 to 90	%	*3
Storage humidity	Hst	10 to 90	%	*3

*1 25 ℃ ±5 ℃

*2 Specified by the highest temperature on the surface.

Available for fan cntrol because the back side temperature of the module assembly can be known via I2C.

*3 No condensation.

Electrical Specifications

Electrical Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply input voltage	V_+9 V	8.0	8.5	9.0	V	
	V_+5 V	4.75	5.0	5.25	V	
Power supply input current	I_+9 V	−	−	0.95	A	*1

	I_+5 V	—	—	0.70	A	
I2C control clock frequency	Clk_I2C	—	—	100	kHz	*2
I2C control High threshold voltage	I2C_SDA,SCL・・・	2.0	—	—	V	
I2C control Low threshold voltage	I2C_SDA,SCL・・・	—	—	0.8	V	

*1 FR; 60 Hz, V_+9 V = 8.0 V, V_+5 V = 4.75 V, 25 ℃±5 ℃, when displaying all white
*2 All control pins in CN105

Interface Connector Specifications

List of Used Connector

Reference	Description	Manufacturer name/model name
CN100	21-pin connector for LVDS signal input	JAE/ FI-RE-21S-HF or equivalent
CN101	10-pin connector for power supply input	JST/ SM010B-GHS-TB(LF)(SN) or equivalent
CN105	8-pin connector for panel module control	JST/ SM08B-GHS-TB(LF)(SN) or equivalent

Pin description of each connector

CN100

Pin No.	Symbol	I/O	I/O voltage range	Description
1	GND	—	GND	Panel GND
2	GND	—	GND	
3	GND	—	GND	
4	RA-	I	1.25 V ± 0.175 V (typ.)	LVDS differential signal
5	RA+	I	1.25 V ± 0.175 V (typ.)	
6	GND	—	GND	Panel GND
7	RB-	I	1.25 V ± 0.175 V (typ.)	LVDS differential signal
8	RB+	I	1.25 V ± 0.175 V (typ.)	
9	GND	—	GND	Panel GND

10	RC-	I	1.25 V ± 0.175 V (typ.)	LVDS differential signal
11	RC+	I	1.25 V ± 0.175 V (typ.)	
12	GND	—	GND	Panel GND
13	RCLK-	I	1.25 V ± 0.175 V (typ.)	LVDS differential signal
14	RCLK+	I	1.25 V ± 0.175 V (typ.)	
15	GND	—	GND	Panel GND
16	RD-	I	1.25 V ± 0.175 V (typ.)	LVDS differential signal
17	RD+	I	1.25 V ± 0.175 V (typ.)	
18	GND	—	GND	Panel GND
19	RE-	I	1.25 V±0.175 V (typ.)	LVDS differential signal
20	RE+	I	1.25 V±0.175 V (typ.)	
21	GND	—	GND	Panel GND

CN101

Pin No.	Symbol	I/O	I/O voltage range	Description
1	+9 V	I	+8.5 V (typ.)	Panel power supply
2	+9 V	I	+8.5 V (typ.)	
3	+9 V	I	+8.5 V (typ.)	
4	GND	—	GND	Panel GND
5	GND	—	GND	
6	GND	—	GND	
7	GND	—	GND	
8	5V	I	+5.0 V (typ.)	Panel power supply
9	5V	I	+5.0 V (typ.)	
10	5V	I	+5.0 V (typ.)	

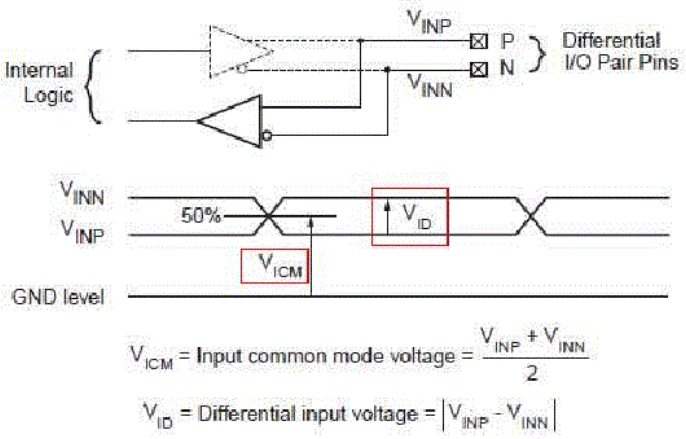
CN105

Pin No.	Symbol	I/O	I/O voltage range	Description
1	I2C_SDA	I/O	0 V to -3.3 V	I2C bus SDA signal
2	I2C_SCL	I	0 V to -3.3 V	I2C bus SCL signal
3	GND	—	GND	Panel GND
4	READY	O	0 V to -3.3 V	READY output signal of panel CPU
5	CONTROL_MODE	I	0 V to -3.3 V	Normally connected to GND
6	RECONFIG	I	0 V to -3.3 V	Restartup control signal of panel CPU
7	GND	—	GND	Panel GND
8	RESERVE			Not available

* CN102 and CN104 on the board are not used.

LVDS input specifications

Differential I/O Standards



Recommended operating setting condition of differential signal

IO Standard Attribute	VCCO for Drivers			VID			VICM		
	Min. (V)	Nom. (V)	Max. (V)	Min. (mV)	Nom. (mV)	Max. (mV)	Min. (V)	Nom. (V)	Max. (V)
LVDS_33	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35

Skew between LVDS clock and data

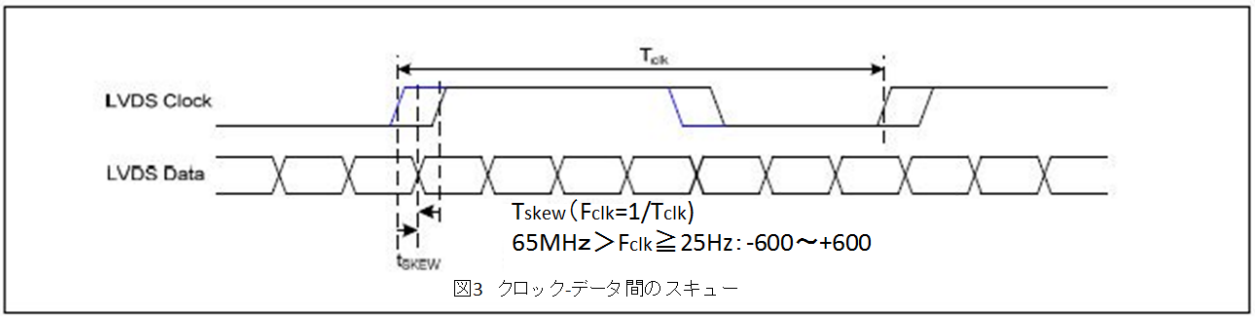


図3 クロック-データ間のスキュー

Item	Symbol	Min.	Max.	Unit	Remarks
LVDS Clock to Data Skew Margin	tskew	-600	+600	ps	65 MHz>Fclk≥25 MHz
LVDS Clock to Clock Skew Margin（Even to Odd)	tskew_EO	-1/7	+1/7	Tclk	
Maximum deviation Of input clock frequency during SSC	FDEV	—	±3	%	
Maximum modulation frequency of input clock during SSC	FMOD	—	200	kHz	

Input Signal Timing

Specification		Minimum	Typical	Max	Unit
Clock	Pixel Clock		41		MHz
Horizontal	Htotal	-	1169	-	dot clk
	Hact	-	960	-	
	H_FP		96		
	H_BP	-	97	-	
	Hsync	-	16	-	
	H polarity		Positive		
	Hfreq	34.547	35.073	35.599	kHz
Vertical	Vtotal	-	584/702/730	-	line
	Vact	-	540	-	
	V_FP		12/130/158		
	V_BP	-	30	-	
	Vsync	-	2	-	
	V polarity		Positive		
	Vfreq	-1.5%	60.057/49.962/48.045	+1.5%	Hz

See the timing table on the next page onward.

* When SYNC_MODE is in HVsync mode.

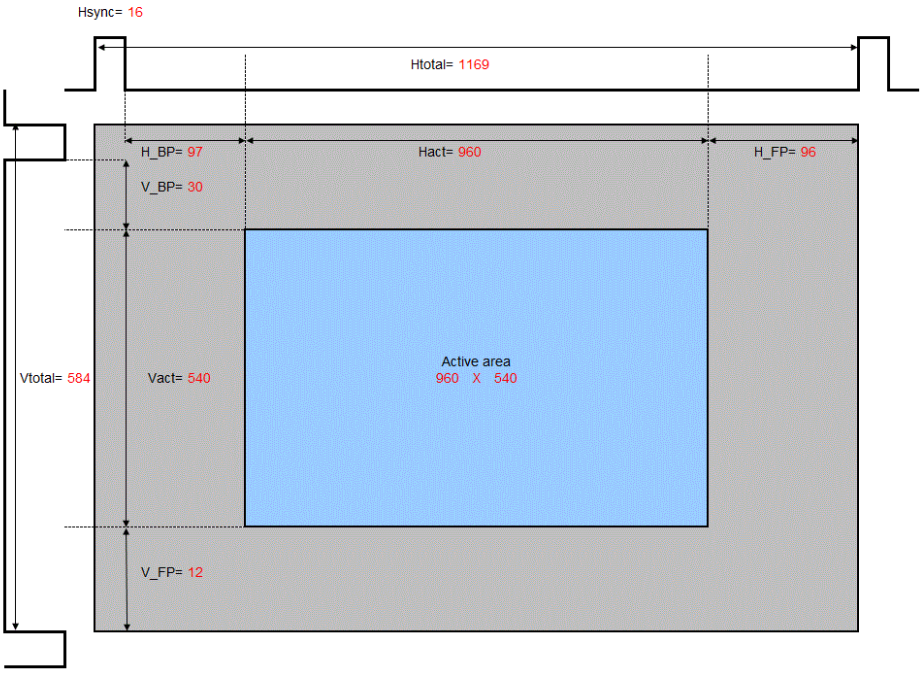
* Change also the register needed to drive it using I2C when changing vertical frequency.

Input Signal Timing

Input Timing 【60Hz】Tcon入力

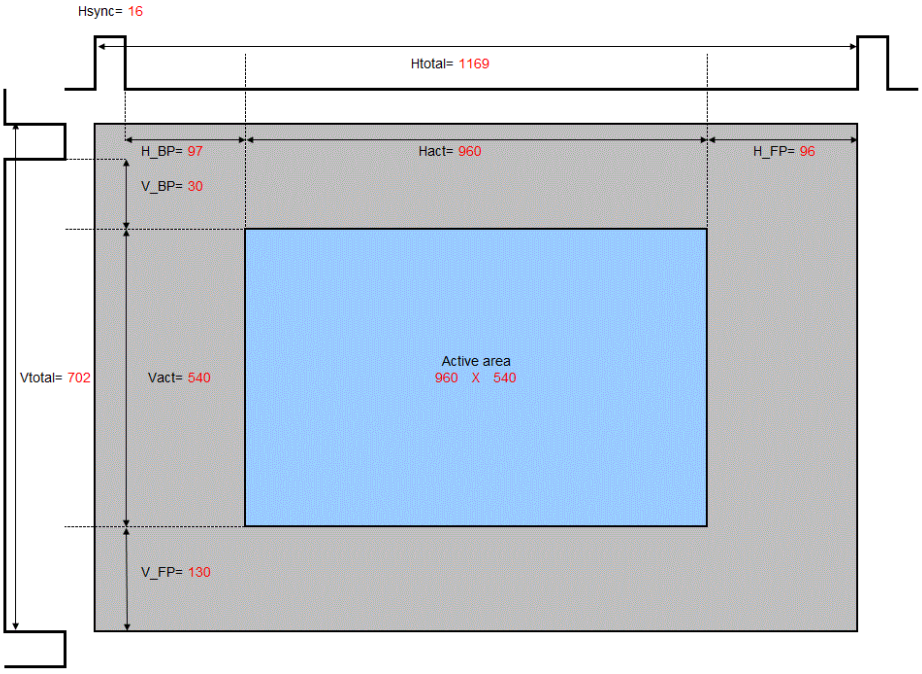
Panel Siz	960 X 540		
Pixel CLK	41	MHz	24.39 ns
Htotal	1169	dot	28.512 us
Hact	960		23.415 us
H_FP	96		2.341 us
H_BP	97		2.366 us
Hsync	16		0.39 us
H polarity	Positive		
Hfreq	35.073	kHz	
Vtotal	584	line	16.651 ms
Vact	540		15.397 ms
V_FP	12		0.342 ms
V_BP	30		0.855 ms
Vsync	2		0.057 ms
V polarity	Positive		
Vfreq	60.057	Hz	

※赤字は固定値
fHが変わらないようにH_FP, H_BP, CLKを決める



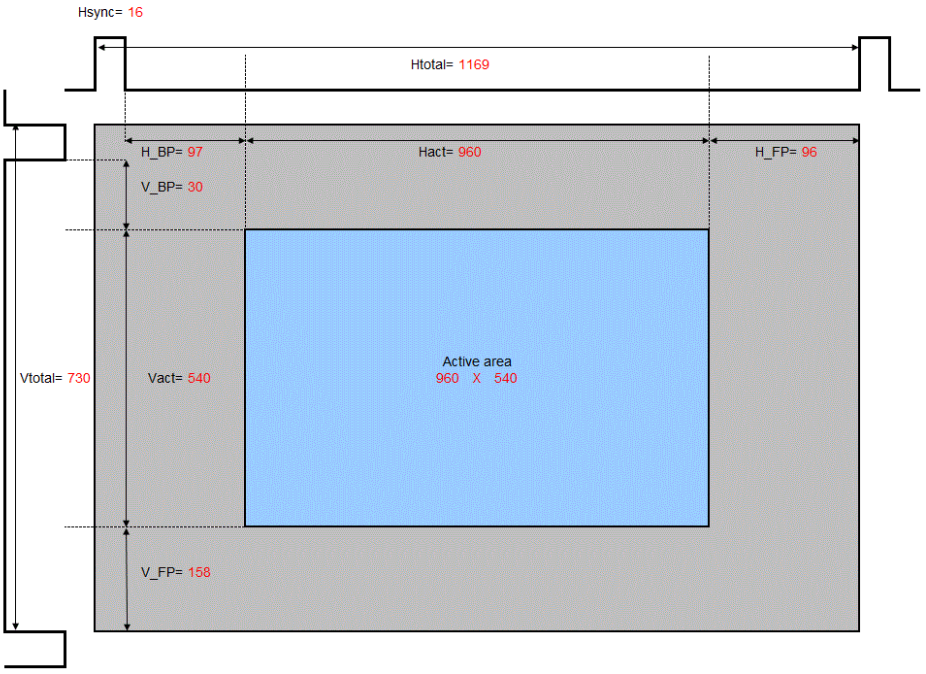
Input Timing 【50Hz】Tcon入力

Panel Siz	960 X 540		
Pixel CLK	41	MHz	24.39 ns
Htotal	1169	dot	28.512 us
Hact	960		23.415 us
H_FP	96		2.341 us
H_BP	97		2.366 us
Hsync	16		0.39 us
H polarity	Positive		
Hfreq	35.073	kHz	
Vtotal	702	line	20.016 ms
Vact	540		15.397 ms
V_FP	130		3.707 ms
V_BP	30		0.855 ms
Vsync	2		0.057 ms
V polarity	Positive		
Vfreq	49.962	Hz	



Input Timing 【48Hz】Tcon入力

Panel Size	960 X 540		
Pixel CLK	41	MHz	24.39 ns
Htotal	1169	dot	28.512 us
Hact	960		23.415 us
H_FP	96		2.341 us
H_BP	97		2.366 us
Hsync	16		0.39 us
H polarity	Positive		
Hfreq	35.073	kHz	
Vtotal	730	line	20.814 ms
Vact	540		15.397 ms
V_FP	158		4.505 ms
V_BP	30		0.855 ms
Vsync	2		0.057 ms
V polarity	Positive		
Vfreq	48.045	Hz	



Display Gray Scale and Input Data Signal

Color \ Input		Red Data								Green Data								Blue Data							
		R9	R8	R7	•••	R3	R2	R1	R0	G9	G8	G7	•••	G3	G2	G1	G0	B9	B8	B7	•••	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red (1022)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1022)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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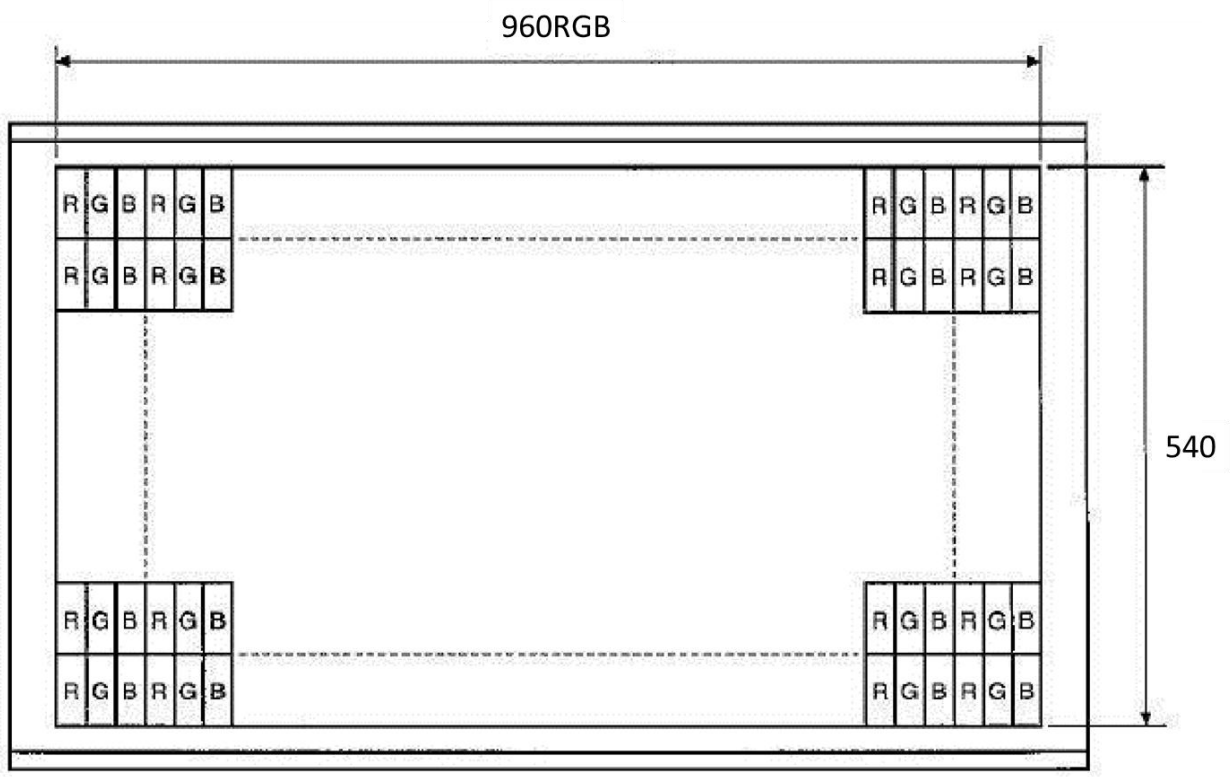
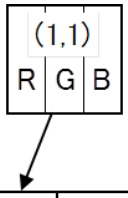
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

* 1 shows High, and 0 shows Low.

* For gray scale (n), the larger n is the brighter the color is.

Pixel data array in display area





(1,1)	(2,1)	(3,1)	(4,1)			(959,1)	(960,1)
(1,2)	(2,2)						
(1,3)	(2,3)						
(1,4)	(2,4)						
(1,540)	(2,540)					(959,540)	(960,540)

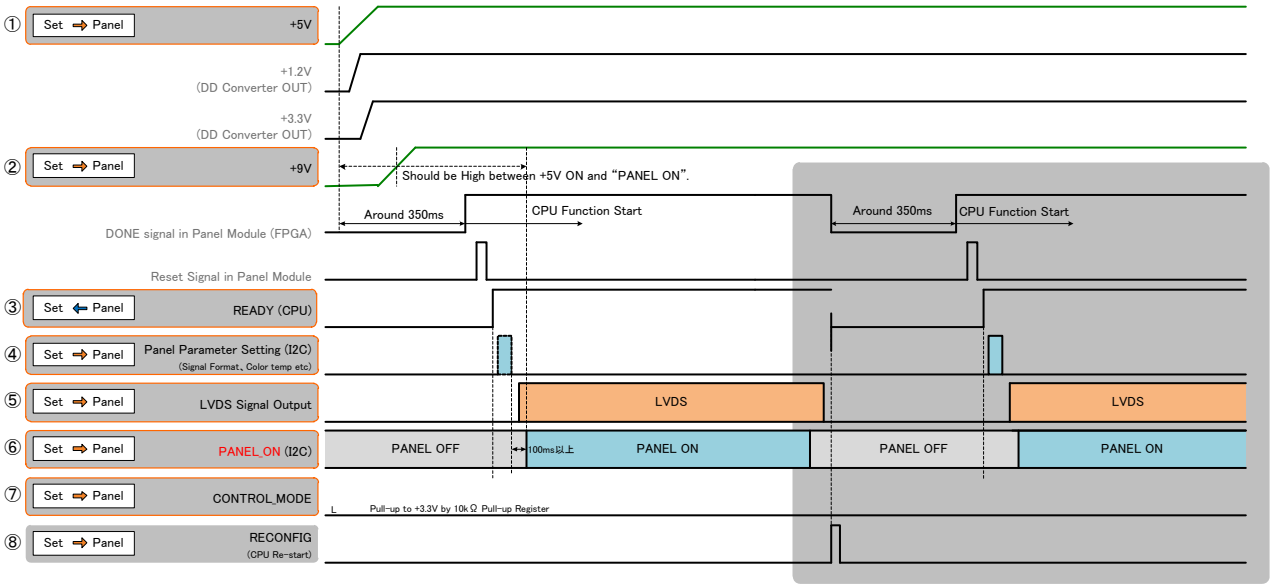
LVDS mapping

LVDS data	Pixel data	Input connector
TA0	R4	RA- RA+
TA1	R5	
TA2	R6	
TA3	R7	
TA4	R8	
TA5	R9	
TA6	G4	
TB0	G5	RB- RB+
TB1	G6	
TB2	G7	
TB3	G8	
TB4	G9	
TB5	B4	
TB6	B5	
TC0	B6	RC- RC+
TC1	B7	
TC2	B8	
TC3	B9	
TC4	HSYNC	
TC5	VSYNC	
TC6	DE	
TD0	R2	RD- RD+
TD1	R3	
TD2	G2	
TD3	G3	
TD4	B2	
TD5	B3	
TD6	-	
TE0	R0	RE- RE+
TE1	R1	
TE2	G0	
TE3	G1	
TE4	B0	
TE5	B1	
TE6	-	
CLK	CLK	RCLK- RCLK+

Power Supply Sequence

Power-on Sequence (I2C control)

POWER ON Sequence



RECONFIG Function

Control Step

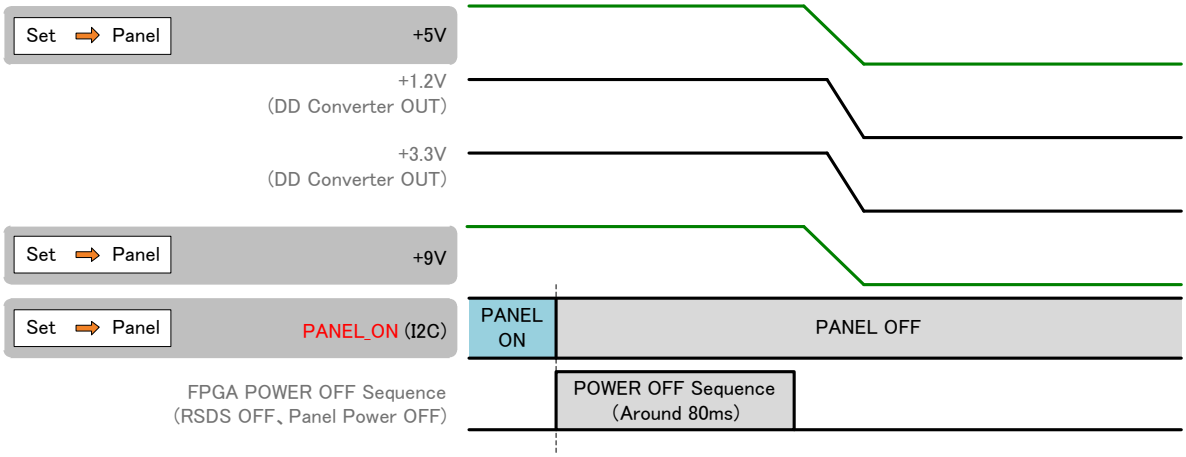
1) 5pin of CN105(CONTROL_MODE) to be 0[V]. ---- ⑦
   Grounding by set side.
2) Power supply to panel module. ---- ①②
   Power supply sequence is, at first +5V and +9V later. Otherwise, at the same timing for both +5V and +9V.
3) Wait until when receiving READY signal from Panel Module.---- ③
4) Writing initial register value for panel parameter via I2C interface. ---- ④
5) LVDS Signal Output. ---- ⑤
6) Panel ON. ---- ⑥
7) If panel module don't work correctly, it is available to re-start CPU with plus pulse to 6pin of CN105(RECONFIG).

CPU Re-start

It is available to re-start CPU with plus pulse to 6pin of CN105(RECONFIG). ---- ⑧
After CPU Re-start, please proceed Step 3) onward.

POWER OFF Sequence

In case for panel power off timing can be controlled by I2C interface.



Control Step

1) In case that panel power off timing can be controlled.
Step1) "Panel Off" by I2C interface and stay around 80msec.
Step2) Power supply off, +5V and +9V.

2) In case that panel power off timing can NOT be controlled.
Highly recommend that power off with +9V at first, and then power off +5V later.

Panel Control Method (I2C)

Changing the setting below via I2C enables the panel characteristics control.

Register Table and the Function

Register description

I2C Bus slave address - Read : 61h, Write : 60h

Name	Function	Bit	R/W	Address	Bit assign 7	6	5	4	3	2	1	0	Default	Description	Register has to be set at initial setting.
PANEL_ON	Panel ON/OFF control.	1	R/W	10h								0	0	[0] Panel off [1] Panel on	Needed to execute when Panel On and Off.
MUTE	Muting Display.	1	R/W	11h								0	0	[0] Normal display [1] Mute	
V_FREQ	Vertical scan frequency setting	2	R/W	12h							1	0	0	[0] 60Hz [1] 50Hz [2] 48Hz [3] Reserved	Needed to select one frequency.
COLOR_SPACE	Color Space Setting	3	R/W	13h						2	1	0	0	[0] Panel native [1] EBU [2] SMPTE-C [3] ITU-R.BT709 [4]-[7] Reserved	Needed to select one color setting.
COLOR_TEMP	Color Temperature Setting	3	R/W	14h						2	1	0	0	[0] D65 [1] D93 [2] Panel native [3]-[7] Reserved	Needed to select one Color Temperature.
SYNC_MODE	SYNC MODE setting.	1	R/W	16h								0	0	[0] DE only mode[Test purpose only] [1] HVsync mode	Please select [1].
T_B_REVERSE	Reverce display, top and bottom.	1	R/W	17h								0	0	Top/Bottom reverse [0] Normal [1] Reverse	Needed to select one.
L_R_REVERSE	Reverce display, right and left.	1	R/W								0		0	Left/Right reverse [0] Normal [1] Reverse	Needed to select one.
PANEL_TEMP	Make sure panel temperature.	9	R	1Ah	7	6	5	4	3	2	1	0		Panel temperature 0.5 degree C/1LSB (2's complement) 0FAh : +125 degree C 000h : 0 degree C 192h : -55 degree C	
				1Bh								8			
OPERATION_TIME	Make sure OperationTime	16	R	46h	7	6	5	4	3	2	1	0		Operation time	
				47h	15	14	13	12	11	10	9	8			
SG_PATTERN	Display with internal display image.	4	R/W	4Eh	3	2	1	0					0	Test pattern [0] External signal (LVDS input) [1] 100% White [2] 100% Red [3] 100% Green [4] 100% Blue [5] 100% ColorBar [6] H Ramp [7] V Ramp [8] Frame [9] Window [10] 80% Gray [11] 60% Gray [12] 40% Gray [13] 20% Gray	

Notes on changing I2C setting)

・Noise or image disturbance in the display area may be seen when setting the register below.

Internal signal display (during signal switching)/panel color range setting/panel color temperature setting/reversed display in up-down direction/reversed display in right-left direction

・SYNC_MODE is set to "0" in the intial setting. Use it under the condition that Hvsync mode is set to "1". When not setting it Sony does not guarantee the normal operation.

I2C Communication Specification

Packet Specification

Write-packet (BE Micro -> Panel Micro)

The packet length is variable and the start subaddress can be set freely. The configuration is shown below.

Start	Slave Address(W)	ACK	Sub Address	ACK	Data1	ACK	・・・	DataN	ACK	STOP

Slave Address(W)	60h
Sub Address	The first address to write (1 Byte)
Data1～DataN	Writing data (Maximum “N” is 15.)
ACK	Acknowledgement

Read-packet (Panel Micro -> BE Micro)

The packet length is variable and the start subaddress can be set freely. The configuration is shown below.

Start	Slave address(W)	ACK	Sub Address	ACK	Start	Slave address(R)	ACK	Data1	ACK	・・・

・・・	DataN	NAK	STOP

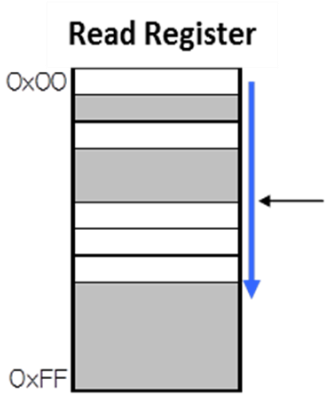
Slave Address(W)	60h
Sub Address	The first address to read (1 Byte)
Slave Address(R)	61h
Data1～DataN	Reading data
ACK	Acknowledgement
NAK	No Acknowledgement

Time interval between packets

The interval between the end of command packet and the start of the following command packet (start condition) should be 500 μs or more.

Processing when accessing undefined area

The processing when accessing undefined area is shown below.

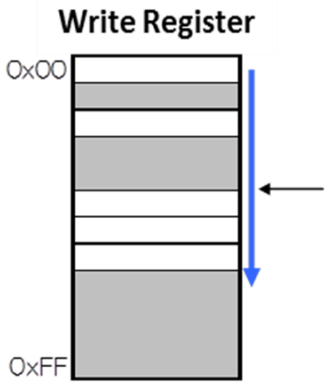


Reading data regulation

・・・ Defined register on p15. Read data on buffer.

・・・ Not defined register on p15. Ignore and no read.

In case accessing in serial for both Defined and Not defined register, Reading data regulation is valid for each register, regardless of starting register.



Writing data regulation

・・・ Defined register on p15. Write data on buffer.

・・・ Not defined register on p15. Write just Zero.

In case accessing in serial for both Defined and Not defined register, Writing data regulation is valid for each register, regardless of starting register.

Timeout

The communication becomes invalid to release all path if the communication does not end (path is still busy) even 500 ms after the time when the last slave address is designated for fail safe.

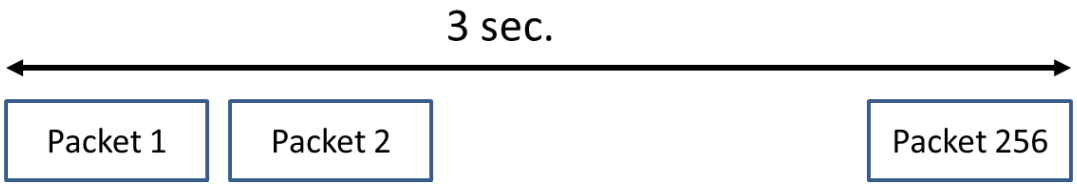
(The I2C device is reset internally.)

Therefore, end all communication within 500 ms after the last slave address is designated to issue the STOP condition.

Restriction on number of commands in 3 second units

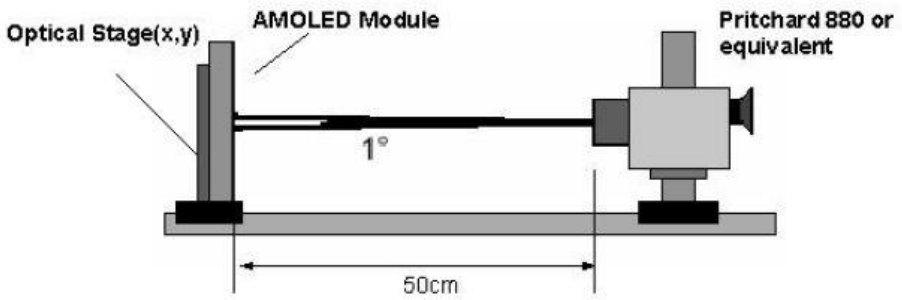
The number of write commands should be 256 or less in any 3 second width.

Remarks: The number of read commands has no restriction due to no queuing.



Optical characteristics

It is measured in the optical system shown below using the optical measurement unit equivalent to CS2000 after the aging of 20 min in darkroom. The drive condition of OLED panel is shown below.



<Panel drive condition>

Ta = 25 ± 2 deg.C, V9v = 8.5 V, V5v = 5 V, fv = 60 Hz

Color temp = D65, Color Space

= panel native setting

Before shipping

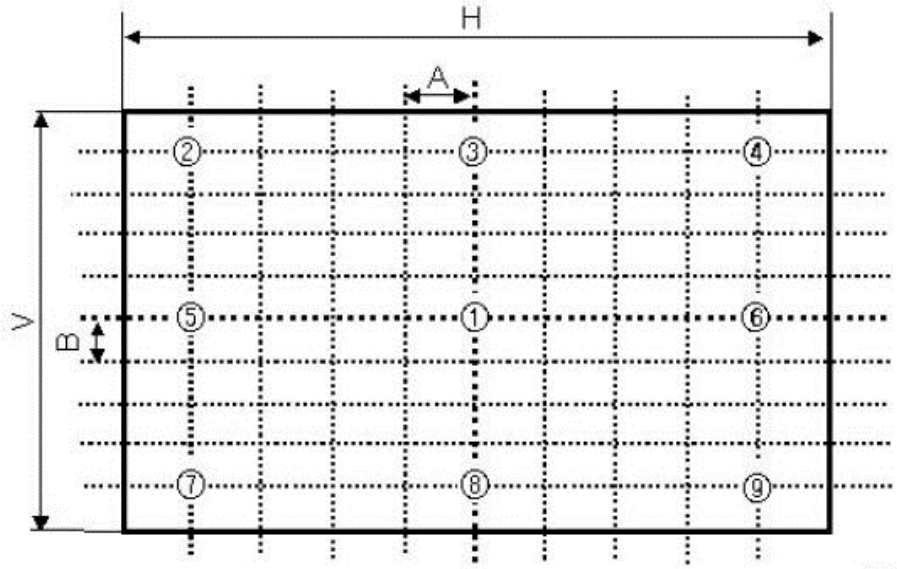
Item		Min.	Typ.	Max.	Unit	Remarks
Luminance	All white	200		250	cd/m^2	*1
	Peak luminance	350				

Luminanceuniformity		9 points	80%				*2
Contrast		Center		100,000		-	*3
Chromaticity	W	x	-0.010	0.313	+0.010	-	*4
		y		0.329		-	
	R	x	0.673	0.681	0.689	-	*5
		y	0.311	0.319	0.327	-	
	G	x	0.17	0.206	0.242	-	
		y	0.718	0.735	0.752	-	
	B	x	0.13	0.135	0.14	-	
		y	0.05	0.062	0.074	-	

*1 When displayiing gray scale of 1023 ABL is ON during Window.

*2 Calculated by the measurement value on the 9 points in the active area below based on the formula below.

Luminance UF ＝ Min. (L1, L2, L3・・・L9)/Max. (L1, L2, L3・・・L9)



A: H/10 mm
B: V/10 mm
@ H,V: Active Area

*3 Calculated by the formula below.

Contrast = Luminance displaying Window in 1023 gray scale/Luminance displaying Window in 0 gray scale

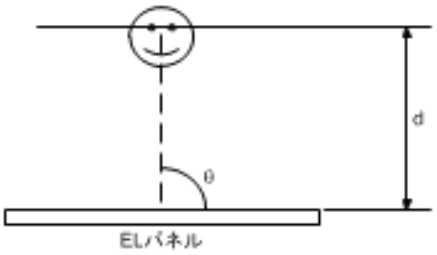
*4 At default value of D65 in the color temperature setting

*5 At default value of Panel Native in the color range setting

Defect Standards

1. Visual Inspection Conditions

The defect of EL panel is inspected visually under the condition below if not any proviso in the respective items.



Inspection Environment and Conditions

Parameter	Conditions
d	3 V (3 times the on-screen vertical dimension)
Panel luminance	0 to 200 cd/m^2
Ambient temperature	25 deg.C (typ.)
Ambient illuminance	100 lx (When lighted) 1100 to 1500 lx (When not lighted)
θ	90 ±5 deg.

2. Defect Standards

2-1. Pixel and Circuit Defects

Item	Total	Distance between adjacent defects	
Bright spot	0		Evaluate at an ambient illuminance of 10 lx or less.
Dark spot	See “2-3. Dark Spot Standard”.	Applied according to color.	Evaluated at 200 cd/m^2.
Line defect	0		

2-2. Bright dot defect specification

Bright dot defect is specified with detection threshold values. Pixels that having brighter luminance than these threshold levels on each gray level are judged to be bright dot defect. Bright dot defect has brighter luminance relative to the normal dot luminance. The definition is not same as that of LCD (Liquid Crystal Display), please pay attention.

Bright Defect threshold ; Red = 180 %, Green = 150 %, Blue = 200 %

Pixels that simultaneously satisfy the following conditions should be ignored.

◆ Luminance level: R, G, B 0.8 cd/m^2 or less

- Number of pixels: Unlimited
- Inspection picture: All black display

2-3. Dark dot defect specification.

Dark spot defect is specified with threshold values. Pixels that having lower luminance than these threshold values on each gray level are judged to be dark dot defect. Dark dot defect having low luminance than that of normal pixel.

Dark dot defect threshold : Red = 40 %, Green = 60 %, Blue = 30 %

Allowable number of dark dot defects.

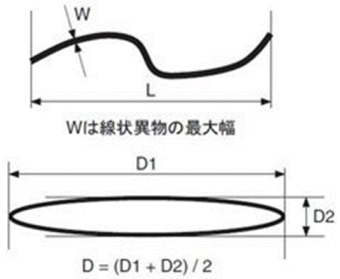
On active display area, should simultaneously satisfy the following condition 1 and 2.

	Red	Green	Blue
Condition 1)	Total number of dark dot defect of R,G,B≦5pcs		
Condition 2)	Total number of dark dot defect of R,G≦3pcs		

2-4. Foreign Matter, Line-shaped Foreign Matter and Air Bubbles

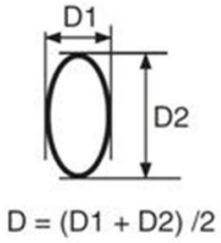
Foreign Matter Standard (Applied to the Light Emitting Area)

Type	Size [mm]		Standard	Distance between adjacent defects	Conditions
Dot-shaped foreign matter	D ≤ 0.2		No Count		Power ON or OFF
	0.2 mm < D ≤ 0.25		2	5 mm or less is rejected.	
	0.25 < D		0		
Line-shaped foreign matter	W ≤ 0.02			No Count	
	0.02 < W ≤0.05	L ≤ 2.0	1	1	
	0.05 < W	2.0 < L	0	0	



Air Bubble Standard

	Size [mm]	Standard	Distance between adjacent defects
Air bubble	D ≤ 0.2	No Count	
	0.2 < D ≤ 0.25	4	5 mm or less is rejected.
	0.25 < D	0	



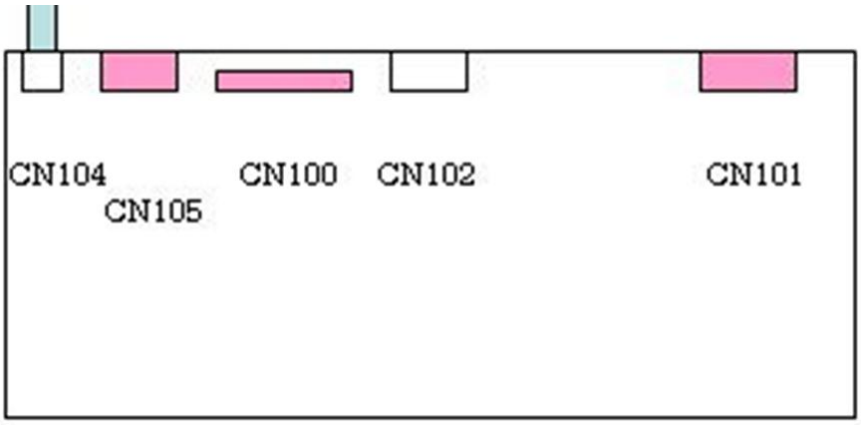
・Mechanical specifications

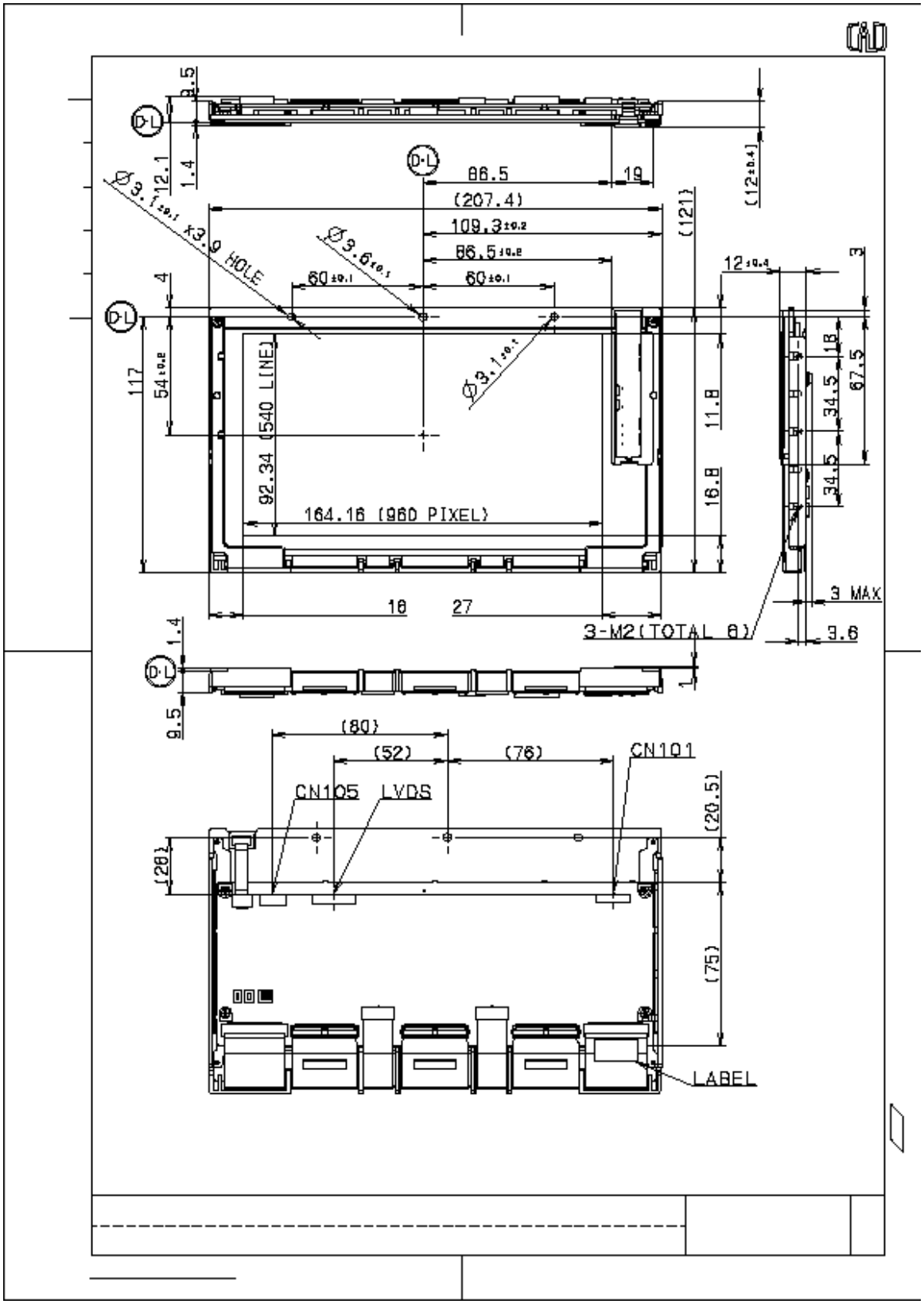
For details, see the appearance on the next page.

Item	Value	
Package dimensions	Horizontal	207.4 mm
	Vertical	121.0 mm

	Thickness	12.0 mm (maximum thickness position 14.6 mm)
Display area	Horizontal	164.160 mm
	Vertical	92.340 mm
Weight	310 g (typ.)	

TCON board



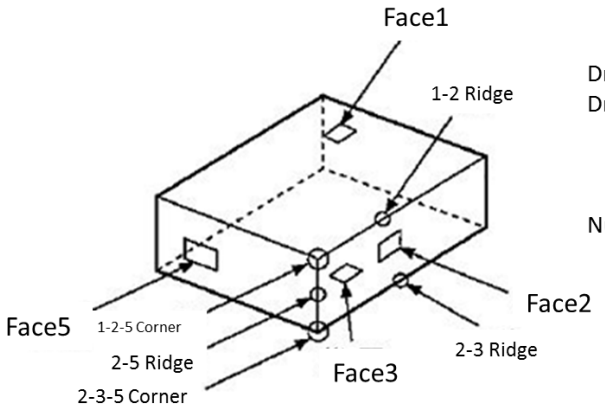

C&D
D-L
3.5
12.1
1.4
Ø3.1±0.1 X3.9 HOLE
Ø3.6±0.1
Ø3.1±0.1
86.5
19
(207.4)
109.3±0.2
86.5±0.2
60±0.1
60±0.1
(121)
(12±0.4)
12±0.4
3
4
117
54±0.2
92.34 (540 LINE)
164.16 (960 PIXEL)
11.8
16.8
18
67.5
34.5
34.5
16
27
3-M2(TOTAL 6)
3 MAX
3.6
1.4
9.5
(80)
(52)
(76)
CN101
CN105
LVDS
(20.5)
(28)
(75)
LABEL

Reliability

Environmental test

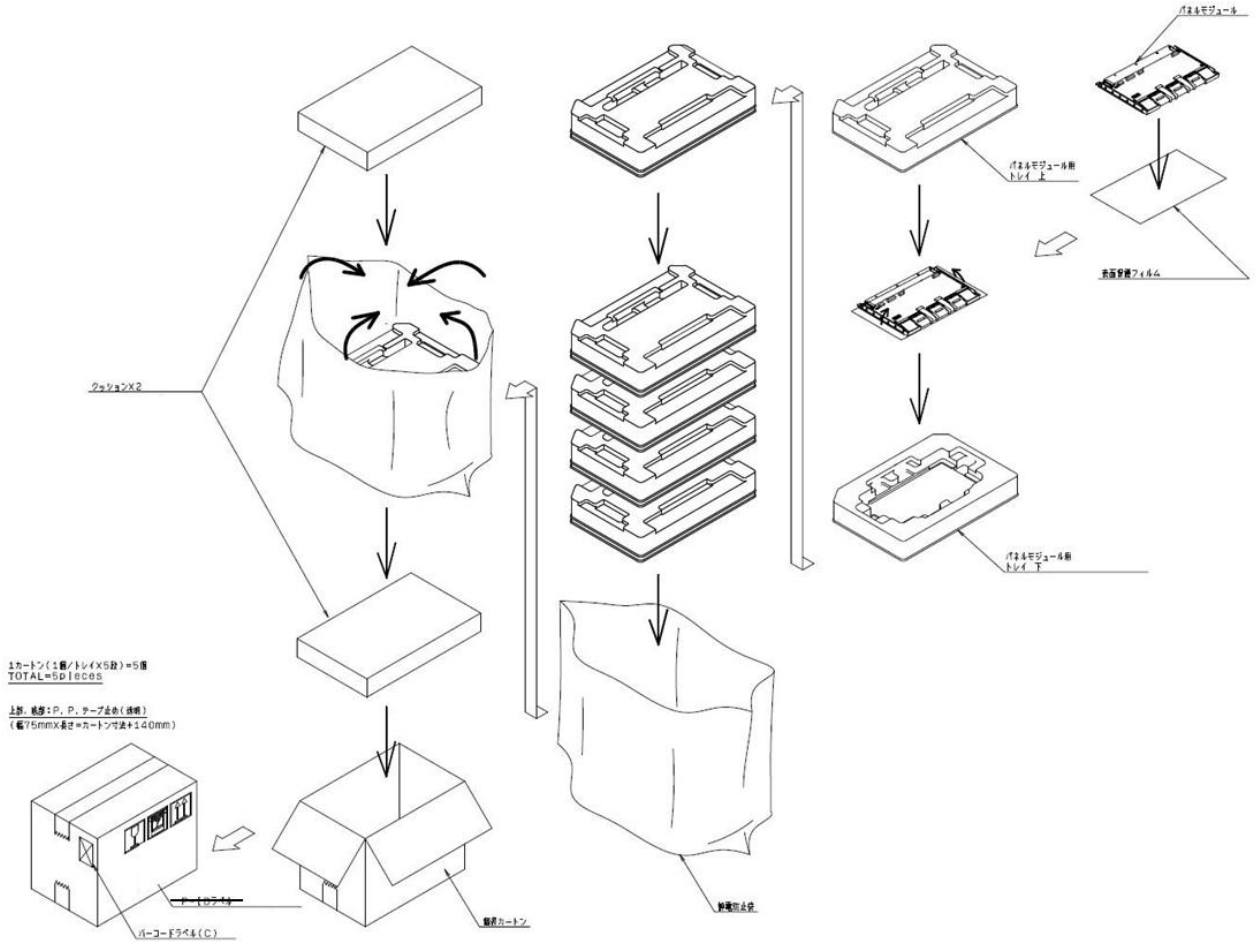
Test item		Conditions		Judgment criteria
Environment	High temperature test	50 °C	Test time: 5 h (operation)	For high temperature and high humidity test, low air pressure and operation test, there should be no problem in operation. For others, there should be no problem in operation and function.
	High temperature & high humidity test	40 °C /95 %	Test time: 48 h (no-operation)	
	Low temperature test	-10 °C	Test time: 5 h (no-operation)	
	Low pressure operation	470 hPa	Operation for 15 minutes or more	
Temperature cycle		-30 to 60 °C	12 h, 2 cyc	
ESD	Surface discharge in air (15 kV)	150 pF/330 Ω	1 cm pitch on the periphery	
Vibration (for packaged products)		20 min, each in the X, Y and Z direction 5 to 50Hz random vibration acceleration: 8.1m/s^2		

Drop test condition



Drop height : 60cm, 50cm, 35cm
Drop condition :
60cm Face 3
50cm Facc2, Face5, 2-3-5 Corner, 2-3 Ridge
35cm 1-2-5 Corner, 1-2 Ridge, 2-5 Ridge
Number of drop
Each 1, total 8 times.

Packing and transportation specification (example)



Notes on Handling

・Take all possible light-shielding steps on the whole PS board (sensor board) so that the entry of external light to the sensor block will be prevented.

・Be sure not to apply external force to PS board. Position change of it may cause display performance that is different from the setting such as ColorTemp.

・Use fixing screws under the specified condition below.

- Side (right-left 3 places) M2 length 4 mm or less (effective screw length inside the module) 0.19 Nm
- Upper (3 places) M3 length 3 mm or more 0.80 Nm

・Be sure not to touch TCP/FPC block, as this may be removed from the panel.

・For the organic electroluminescence panel in general, image retention may occur due to the characteristic of the material that is adopted to realize the high resolution image. To keep displaying fixed image or display it repeatedly at the same position on the screen cannot delete the image that has been retained.

The countermeasure such as avoiding fixed display including character display, setting screen saver function or frequent power-OFF is effective to reduce the image retention.

1. Static charge prevention
   Be sure to take the following protective measures. OLED panels (modules) are easily damaged by static charges.
   (1) Use non-chargeable gloves, use bare hands.
   (2) Use a wrist strap when handling.
   (3) Do not touch any electrodes of the panel.
   (4) Wear non-chargeable clothes and conductive shoes.
   (5) Install grounded conductive mats on the working floor and working table.
   (6) Keep the panel (module) away from any charged materials.
   (7) Use ionized air to discharge the panel (module).

2. Protection from dust and dirt
   (1) Operate in a clean environment.
   (2) Do not touch the AR film surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
   (3) Use ionized air to blow dust off the panel surface.

3. Others
   (1) Do not drop the panel (module).
   (2) Do not twist or bend the panel (module).
   (3) Keep the panel (module) away from heat sources.
   (4) Do not dampen the panel (module) with water or other solvents.
   (5) Do not store or use of the panel (module) at high temperatures or high humidity, as this may affect the characteristics.
   (6) Condensation occurs on the panel (module) when stored in a place where temperature changes rapidly. Store it in a place where temperature changes as small as possible to avoid condensation.